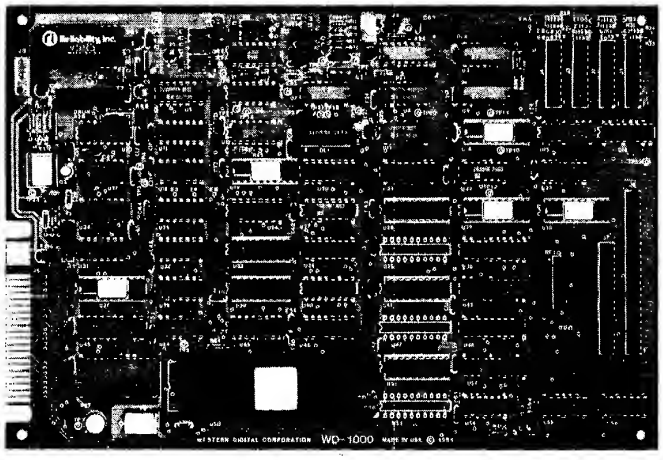
WD1000 Winchester Disk Controller



FEATURES

- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- CRC GENERATION/VERIFICATION
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (ROM SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- 8-BIT HOST INTERFACE
- 0°C to 50°C OPERATION

GENERAL DESCRIPTION

The WD 1000 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive. Either a 34 pin (5¼" drive) or 50 pin (8" drive) connector is provided, as well as four 20 pin data connectors.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro cammands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive.

The WD1000 is based upon a proprietary chip set, the WD1100, specifically designed for Winchester Control.

ORGANIZATION

The WD1000 has seven on board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

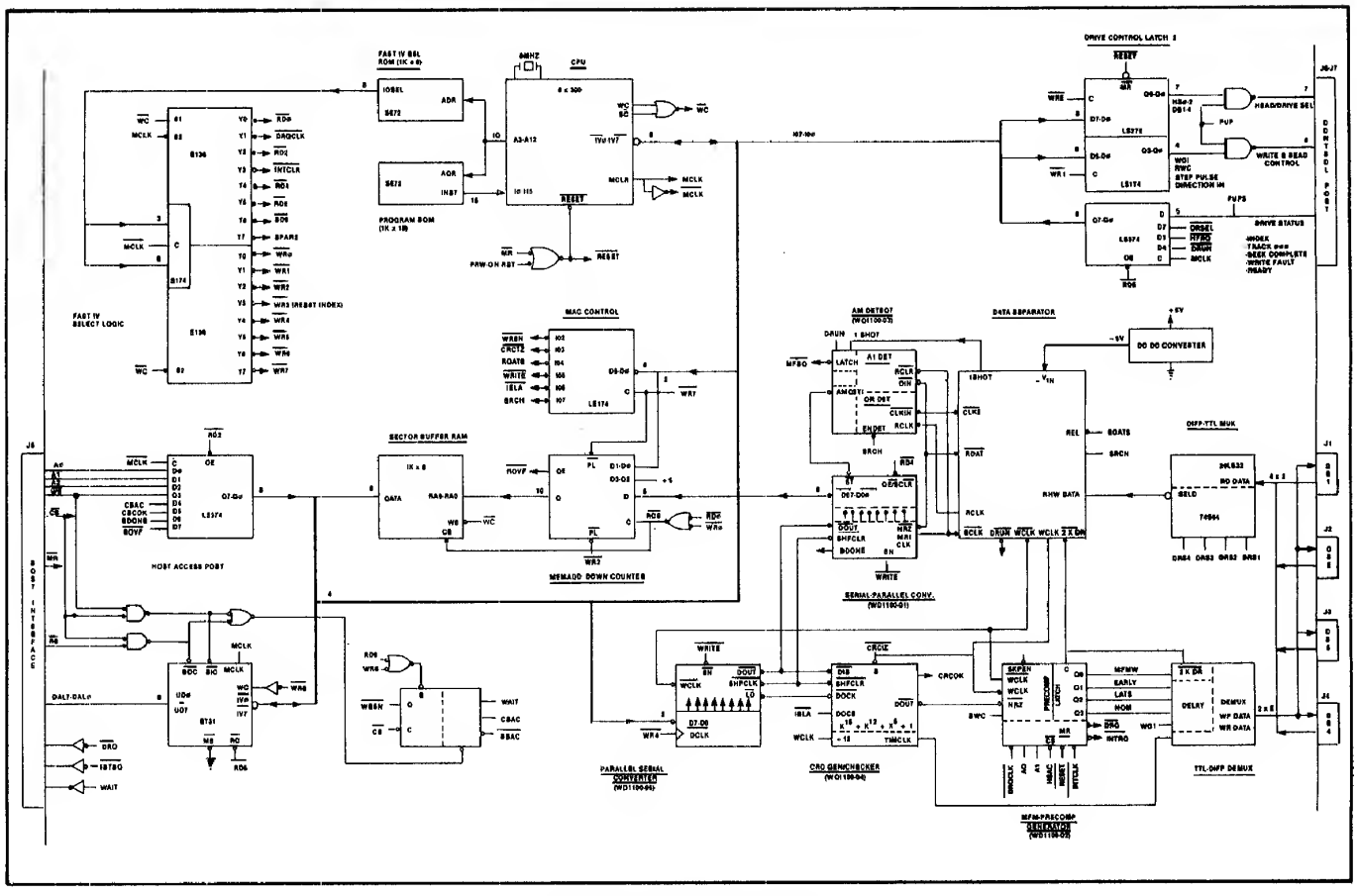
The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1000.

The host interface connector provides interface signals that are compatible with most microprocessors and minicomputers.

WD1100

For those who want to design their own board around the WD1100 chip set, Western Digital can provide schematics, artwork, and programming information. Western Digital also has a complete staff of Applications Engineers to provide additional support. For further information please contact your local representative, or our main plant listed on page 8.



WD1000 BLOCK DIAGRAM

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 uS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec or 5.000 Mbits/sec
Write Precomp Time:	10 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3 M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.) −8 to −18V, 50 mA*
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	9.9 in. (24.9 cm)
Width:	6.8 in. (17.1 cm)
Height:	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)

* Optional −V Supply Available.

HOST INTERFACING

The WD1000 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the $\overline{\text{WAIT}}$ line.

Waits

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1000 is accessing data internally to send to the host during a read operation
- The WD1000 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1000. When the WD1000 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1000 cannot return the requested data within 100 nS, it will assert its $\overline{WAIT}$ line. The period of the $\overline{WAIT}$ signal will vary from 750 nS to 6 uS with 1.25 uS being about average. The period of the $\overline{WAIT}$ only approaches 6 uS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1000 register if that first read or write happens within approximately 6 uS of a command being issued.

During the time that $\overline{WAIT}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The user can modify the timing of the wait signal by selecting a jumper. The WD1000 is shipped with a jumper (or trace) between E4 and E5. This enables waits as soon as the $\overline{CS}$ signal is asserted. This timing is a requirement for some processors and compatible with most. If the host system requires the $\overline{WAIT}$ signal to be asserted only when $\overline{RE}$ or $\overline{WE}$ are asserted in conjunction with $\overline{CS}$, the trace at E4 and E5 should be cut and a jumper should be installed between E4 and E3.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL3 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the host may read data from a selected register of the WD1000.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	−V	Optional −V input from host supplies −8 to −15V to the on-board −5 Volt regulaton (VRI). This power input is also available on J6, pin 2. −V is not required if DC/DC convertor (PSI) is used.
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.

HOST INTERFACE CONNECTOR (Continued)

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exausted or until a write or read is performed on the Cylinder Low register.
40	39	$\overline{MR}$	The Master Reset line initializes all internal logic on the logic on the WD1000. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ line is reset and the INTRQ line is set.
	41	Not Connected	
	42	Not Connected	
	43-50		+5V 8 power pins for regulated +5 volts. This power input is also available on J6, pin 3.
Note: Grounds			Even numbered pins (2-40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1000, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6	O	$\overline{Write\ Gate}$
7	8	I	$\overline{Seek\ Complete}$
9	10	I	$\overline{TR000}$
11	12	I	$\overline{Write\ Fault}$
13	14	O	$\overline{Head\ Select\ 0}$
15	16		NC
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24	O	$\overline{Step}$
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	$\overline{RWC}$
3	4	O	$\overline{Head\ Select\ 2}$
5	6		NC
7	8	I	$\overline{Seek\ Complete}$
9	10		NC
11	12		NC
13	14	O	$\overline{Head\ Select\ 0}$
15	16		NC
17	18	O	$\overline{Head\ Select\ 1}$
19	20	I	$\overline{Index}$
21	22	I	$\overline{Ready}$
23	24		NC
25	26	O	$\overline{Drive\ Select\ 1}$
27	28	O	$\overline{Drive\ Select\ 2}$
29	30	O	$\overline{Drive\ Select\ 3}$
31	32	O	$\overline{Drive\ Select\ 4}$
33	34	O	$\overline{Direction\ In}$
35	36	O	$\overline{Step}$
37	38		NC
39	40	O	$\overline{Write\ Gate}$
41	42	I	$\overline{TR000}$
43	44	I	$\overline{Write\ Fault}$
45	46		NC
47	48		NC
49	50		NC

DRIVE CONTROL SIGNAL DESCRIPTIONS

$\overline{\text{RWC}}$

When the Reduce Write Current line is activated with write gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

$\overline{\text{Write Gate}}$

This output signal allows data to be written on the disk.

$\overline{\text{Seek Complete}}$

Informs the WD1000 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

$\overline{\text{Track 000}}$

Indicates that the R/W heads are positioned on the outermost cylinder. This line is sampled immediately before each step is issued.

$\overline{\text{Write Fault}}$

Informs the WD1000 that some fault has occurred on the selected drive. The WD1000 will not execute commands when this signal is true.

$\overline{\text{HS0}}$ $\overline{\text{HS2}}$

Head Select lines are used by the WD1000 to select a specific R/W head on the selected drive.

$\overline{\text{Index}}$

Is used to indicate the Index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

$\overline{\text{Ready}}$

Informs the WD1000 that the desired drive is selected and that its motor is up to speed. The WD1000 will not execute commands unless this line is true.

$\overline{\text{Step}}$

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the $\overline{\text{SEEK COMPLETE}}$ time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1}}$ $\overline{\text{DS4}}$

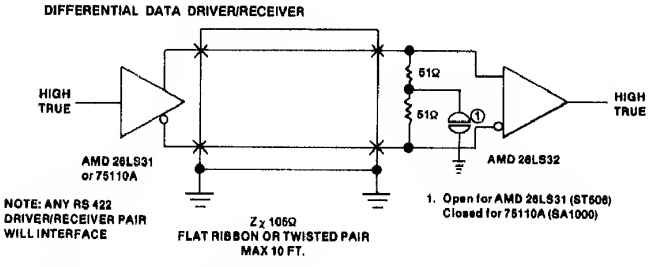
These four Drive Select lines are used to select one of four possible drives.

DRIVE DATA CONNECTOR

Four data connectors (J1-4) are provided for clock signals and data between the WD1000 and each drive. All lines associated with the transfer of data between the drive and the WD1000 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

DATA CONNECTIONS AND DESCRIPTIONS **TABLE 4**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock
	10	O	– Timing Clock
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM READ DATA
	18	I	– MFM READ DATA
19			GND
20			GND



POWER CONNECTOR

A three pin molex connector (J6) is provided for power input to the board. The customer supplied mating connector housing is Molex 03-09-1032. The pin-outs are as shown in Table 5:

TABLE 5

PIN	SIGNAL NAME
1	GROUND
2	– 8 to – 15 V unregulated
3	+ 5 V regulated

COMMANDS

The WD1000 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1000 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data CRC errors. If the R/W head mis-positions, the WD1000 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1000 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1000 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized In Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	D	0	0	0
III	Write Sector	0	0	1	1	0	0	0	0
III	Format Track	0	1	0	1	0	0	0	0

r3-r0 — STEPPING RATE

0000 = 10uS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode
0 = Programmed I/O Mode
1 = DMA Mode

NOTE:

The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TR000 line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The TR000 line is sampled. If TR000 is true, an interrupt is generated and the Busy bit is reset. If TR000 is not true, stepping pulses at a rate determined by the stepping rate field are issued until the TR000 line is activated. When TR000 is activated, the Busy bit is reset and an interrupt is issued. If the TR000 line is not activated within 1023 stepping pulses, the TR000 Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylinder to be read and an interrupt is issued. Note that the Seek Complete line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1000 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1000 will attempt to read the sector. The WD1000 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC, if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred a data CRC error.

Every time the controller encounters an error, it records the occurance of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Data CRC Error bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1000 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upon receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1000 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

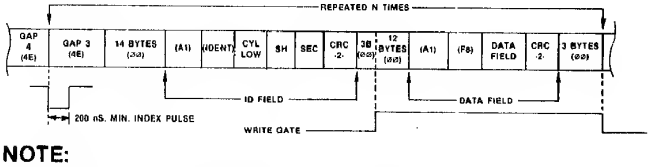
If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high These values are:
   - FE = 0 to 255 cylinders
   - FF = 256 to 511 cylinders
   - FC = 512 to 767 cylinders
   - FD = 768 to 1023 cylinders
6) GAP 4 values are:

SECTOR LENGTH	GAP 3	GAP 4	SECTOR COUNT
128	15	356	54
256	15	352	32
512	30	800	17

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted com-

mand bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.

After the last sector is written, the controller back-fills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1000 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1000 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1000 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessable by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

$\overline{CS}$	A2	A1	A0	$\overline{RE}$	$\overline{WE}$
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

See page 725 for ordering information.

SDH REGISTOR

BIT	7	6 5	4 3	2 1 0
FUNCTION	0	Sec Size	Drive Select	Head Select

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 0
0	1	Drive Sel 1
1	0	Drive Sel 2
1	1	Drive Sel 3

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	CRC Error — Data Field
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	—	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

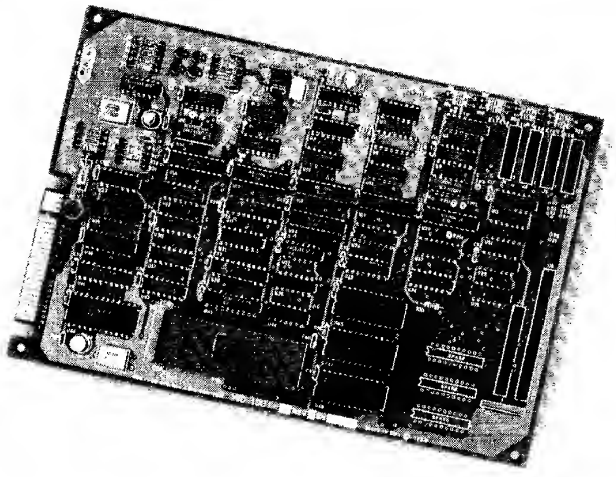
PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1000 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1000. The WD1000 performs all needed retries, even on data CRC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1000 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1000 simulates a normal completion so that special error recovery software is not needed.

Printed in U.S.A.

PRELIMINARY

WD1001 Winchester Disk Controller



GENERAL DESCRIPTION

The WD 1001 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive. Either a 34 pin (5¼" drive) or 50 pin (8" drive) connector is provided, as well as four 20 pin data connectors.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive.

The WD1001 is based upon a proprietary chip series, the WD1100, specifically designed for Winchester Control.

FEATURES

- SINGLE +5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- 32 BIT ECC FOR BURST ERROR CORRECTION
- ERROR CORRECTION ON DATA FIELD ERRORS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD BLOCK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (SOFTWARE SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- 8-BIT HOST INTERFACE
- 0°C TO 50°C OPERATION

ORGANIZATION

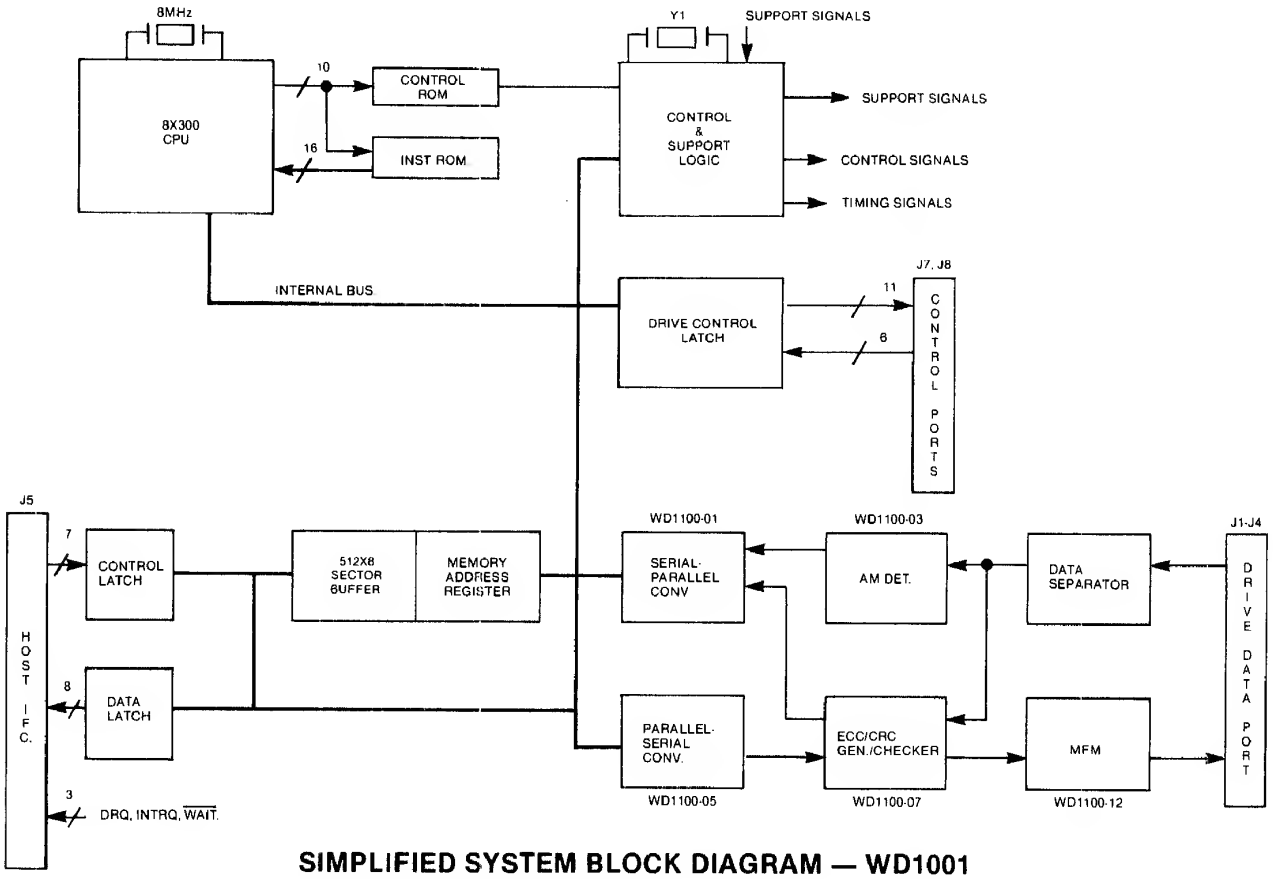
The WD1001 has seven on-board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1001.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

The WD1001 provides dual burst detection and single 5-bit burst correction ECC circuitry. The ECC polynomial has been computer generated for optimum error correction on Winchester Disks.



SIMPLIFIED SYSTEM BLOCK DIAGRAM — WD1001

SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 μS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec or 5.000 Mbits/sec
Write Precomp Time:	12 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1 M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes
Length:	9.9 in. (24.9 cm)
Width:	6.8 in. (17.1 cm)
Height:	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)

HOST INTERFACING

The WD1001 is designed to easily interface to most micro computers and mini-computers. All interfacing is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the WAIT line.

WAITS

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1001 is accessing data internally to send to the host during a read operation.
- The WD1001 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1001. When the WD1001 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1001 cannot return the requested data

within 100 nS, it will assert its $\overline{WAIT}$ line. The period of the $\overline{WAIT}$ signal will vary from 750 nS to 6 μS with 1.25 μS being about average. The period of the $\overline{WAIT}$ only approaches 6 μS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1001 register if that first read or write happens within approximately 6 μS of a command being issued.

During the time that $\overline{WAIT}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the host may read data from a selected register of the WD1001.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1001. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
	41	Not Connected	
	42	Not Connected	
	43-50	+ 5V	8 power pins for regulated + 5 volts. This power input is also available on J6, pin 3.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1001, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TR000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6		NC
7	8	I	Seek Complete
9	10		NC
11	12		NC
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24		NC
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In
35	36	O	Step
37	38		NC
39	40	O	Write Gate
41	42	I	TR000
43	44	I	Write Fault
45	46		NC
47	48		NC
49	50		NC

DRIVE CONTROL SIGNAL DESCRIPTIONS

RWC

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

Write Gate

This output signal allows data to be written on the disk.

Seek Complete

Informs the WD1001 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

Track 000

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

Write Fault

Informs the WD1001 that some fault has occurred on the selected drive. The WD1001 will not execute commands when this signal is true.

HS0 HS2

Head Select lines are used by the WD1001 to select a specific R/W head on the selected drive.

Index

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1001 that the desired drive is selected and that its motor is up to speed. The WD1001 will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

Direction In

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

DS1 DS4

These four Drive Select lines are used to select one of four possible drives.

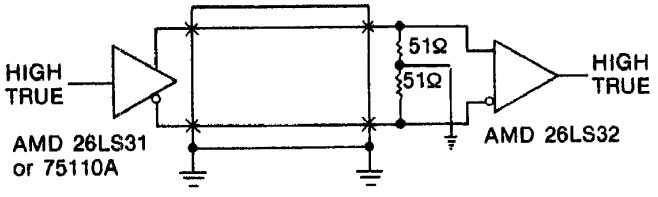
DRIVE DATA CONNECTOR

Four data connectors (J1-4) are provided for clock signals and data between the WD1001 and each drive. All lines associated with the transfer of data between the drive and the WD1001 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

DATA CONNECTIONS AND DESCRIPTIONS **TABLE 4**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock
	10	O	– Timing Clock
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

$Z_\chi = 105\Omega$
FLAT RIBBON OR TWISTED PAIR
MAX 10 FT.

POWER CONNECTOR

A three pin molex connector (J6) is provided for power input to the board. The customer supplied mating connector housing is Molex 03-09-1032. The pin-outs are as shown in Table 5:

TABLE 5

PIN	SIGNAL NAME
1	Ground
2	Not Connected
3	+5 V Regulated

COMMANDS

The WD1001 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1001 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mis-positions, the WD1001 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1001 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1001 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized in Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	D	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r_3-r_0 — STEPPING RATE

0000 = 10μS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode
0 = Programmed I/O Mode
1 = DMA Mode

L = Long Read/Write
0 = Normal Read/Write
1 = Long Read/Write

M = 1 = Multiple Sector Read/Write
0 = Single Sector Read/Write

NOTE:

The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the $\overline{TR000}$ line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{Seek\ Complete}$, $\overline{Ready}$ and $\overline{Write\ Fault}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is rest.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The $\overline{TR000}$ line is sampled. If $\overline{TR000}$ is true, an interrupt is generated and the Busy bit is reset. If $\overline{TR000}$ is not true, stepping pulses at a rate determined by the stepping rate field are issued until the $\overline{TR000}$ line is activated. When $\overline{TR000}$ is activated, the Busy bit is reset and an interrupt is issued. If the $\overline{TR000}$ line is not activated within 1023 stepping pulses, the $\overline{TR000}$ Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of $\overline{Seek\ Complete}$, $\overline{Ready}$ and $\overline{Write\ Fault}$ are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylinder to be read

and an interrupt is issued. Note that the Seek Complete line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1001 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

READ SECTOR

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1001 will attempt to read the sector. The WD1001 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC or if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred an uncorrectable error.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the WD1001 encounters an ECC error, it will attempt to correct the data in its sector buffer. If it can correct the data, the Corrected bit in the Status register will be set, if not, the Uncorrectable Error bit is set.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Uncorrectable bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

READ LONG

This variation of the Read command allows the user to read the ECC check bits directly. The check bits are placed in the data buffer immediately behind the data. This increases the effective buffer length by four bytes.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1001 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upon receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1001 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

WRITE LONG

This variation of the write command allows the user to introduce various error patterns to check correction capability. The check bits follow the data in the sector buffer. This increases the effective buffer length by four bytes.

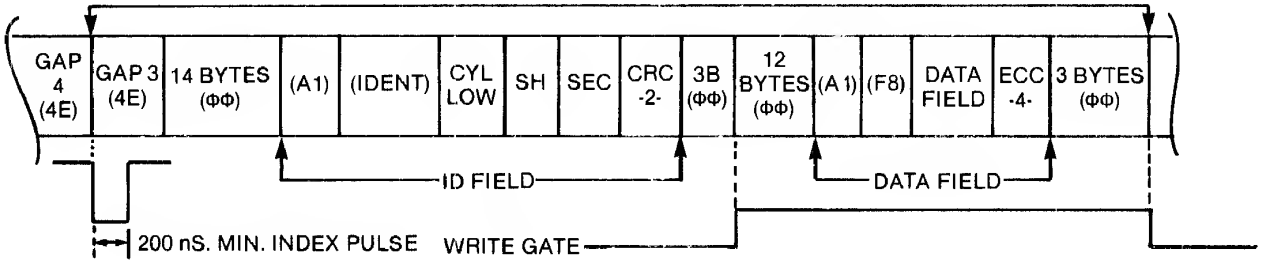
FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted command bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's ECC or CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high These values are:
   - FE = 0 to 255 cylinders
   - FF = 256 to 511 cylinders
   - FC = 512 to 767 cylinders
   - FD = 768 to 1023 cylinders
6) GAP 3 values are:

SECTOR LENGTH	GAP 3
128	15
256	15
512	30

After the last sector is written, the controller backfills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1001 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1001 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1001 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/head	Size/Drive/head
0	1	1	1	Status Register	Command Register

SDH REGISTER

BIT	7	6 5	4 3	2 1 0
FUNCTION	Sec Ext	Sec Size	Drive Select	Head Select

BIT 7	SECTOR EXTENSION
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 0
0	1	Drive Sel 1
1	0	Drive Sel 2
1	1	Drive Sel 3

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	Uncorrectable
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1001 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1001. The WD1001 performs all needed retries, even on data ECC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1001 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1001 simulates a normal completion so that special error recovery software is not needed.

See page 725 for ordering information.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

Printed in U.S.A.

ADVANCE INFORMATION

WD1002 Winchester Disk Controller

GENERAL DESCRIPTION

The WD1002 is next generation of Winchester Controllers. It utilizes the WD1010 Winchester controller chip, and provides for floppy disk back up using the WD279X series of single chip floppy controllers.

Incorporated in this controller is all the circuitry needed for Hard disk control with floppy backup.

The firmware is incorporated in the WD1010 and the controller is compatible with previous WD1000 and WD1001. Additional software is needed for the floppy disk backup. Users of the WD1000/WD1001 need not use the floppy controller.

FEATURES

- SINGLE 5V SUPPLY
- FLOPPY DISK BACKUP
- ECC/CRC
- ST506 OR SA1000 INTERFACE
- COMPACT SIZE
- SECTOR SIZES TO 1024
- DATA RATES TO 5MBS
- AUTOMATIC FORMATTING
- WD1000 COMPATIBILITY

See page 725 for ordering information.

Printed in U.S.A.

WD1100 Series Winchester Controller Chips

DESCRIPTION

The WD1100 Chip series provides a low cost alternative for developing a Winchester Controller. These devices have been designed to read and convert an MFM data stream into 8-bit parallel bytes. During a write operation, parallel data is converted back into MFM to be written on the disk. Address Marks are generated and detected while CRC bytes can be appended and checked on the data stream. The WD1100 is fabricated in N-channel silicon gate technology and is available in a 20-pin Dual-In-Line package.

- WD1100-01 SER/PARALLEL CONVERTER
- WD1100-02 MFM GENERATOR
- WD1100-12 IMPROVED MFM GENERATOR
- WD1100-03 AM DETECTOR
- WD1100-04 CRC GENERATOR/CHECKER
- WD1100-05 PAR/SERIAL CONVERTER
- WD1100-06 ECC/CRC LOGIC
- WD1100-07 HOST INTERFACE LOGIC
- WD1100-09 DATA SEPARATION SUPPORT LOGIC

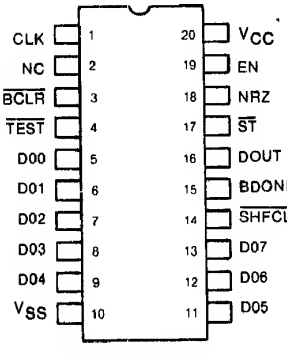
FEATURES

- SA1000/ST506 COMPATIBLE
- SINGLE 5V SUPPLY
- TRI-STATE DATA LINES
- 5 MBITS/SEC TRANSFER RATE
- SIMPLIFIED INTERCONNECT

APPLICATIONS

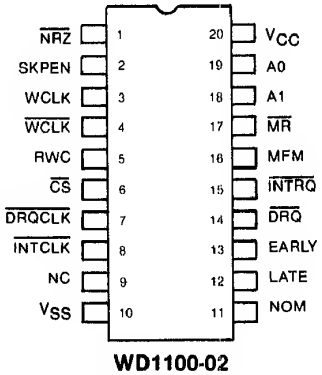
Winchester Controllers For:

- SHUGART ASSOCIATES
- SEAGATE TECHNOLOGY
- QUANTUM CORP.
- TANDON MAGNETICS
- MINISCRIBE
- RMS
- CMI . . . AND OTHERS



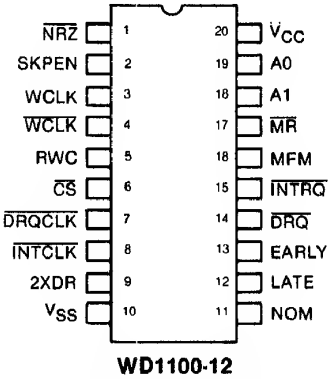
WD1100-01

SERIAL/PARALLEL CONVERTER



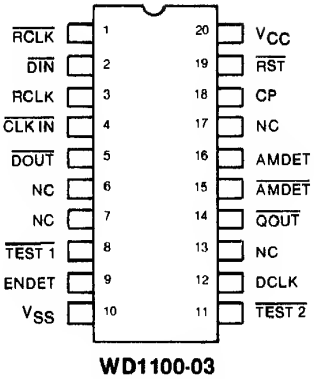
WD1100-02

MFM GENERATOR



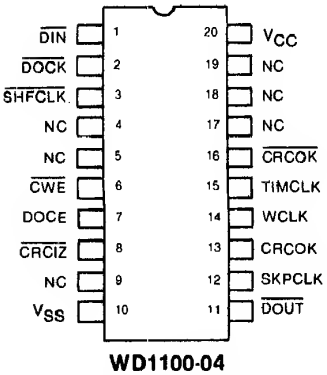
WD1100-12

IMPROVED MFM GENERATOR



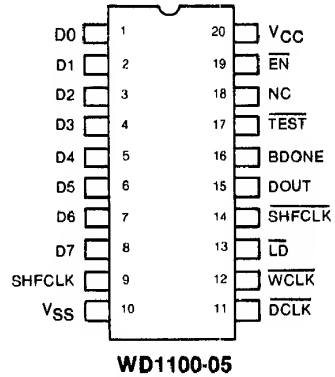
WD1100-03

AM DETECTOR



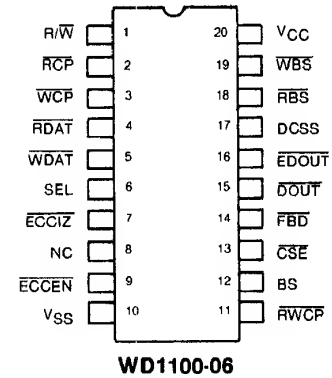
WD1100-04

CRC GENERATOR/CHECKER



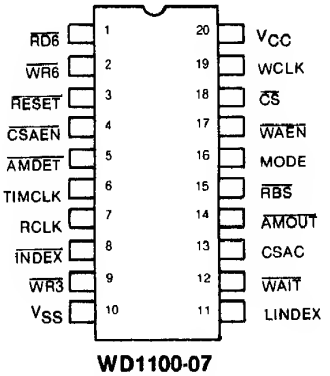
WD1100-05

PARALLEL/SERIAL CONVERTER



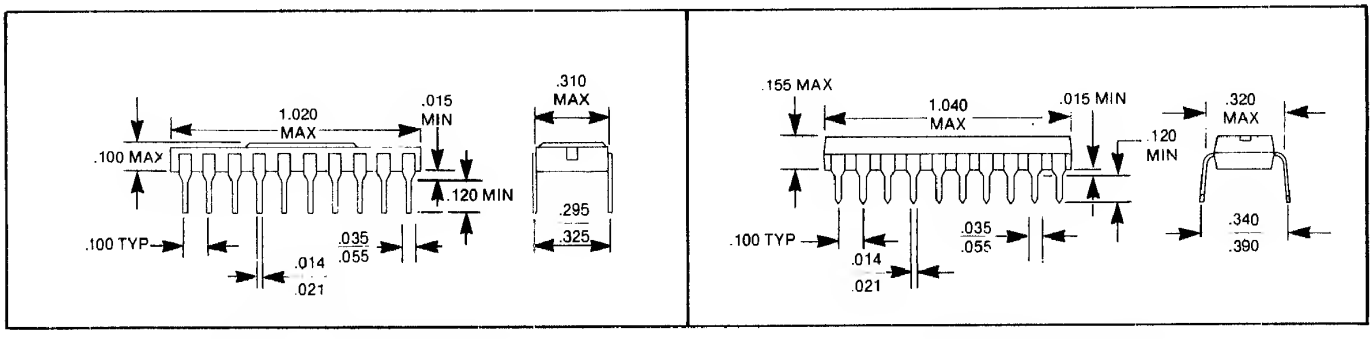
WD1100-06

ECC/CRC LOGIC



WD1100-07

HOST INTERFACE LOGIC



20 LEAD CERAMIC "U"

20 LEAD PLASTIC 'V"

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-01 Serial/Parallel Converter

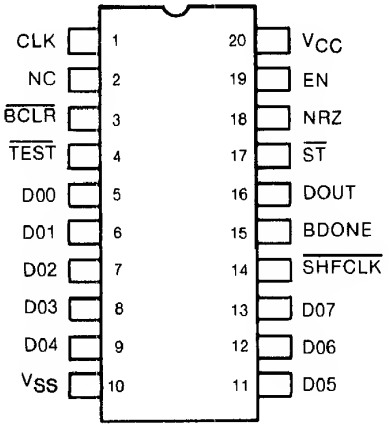
DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8 bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

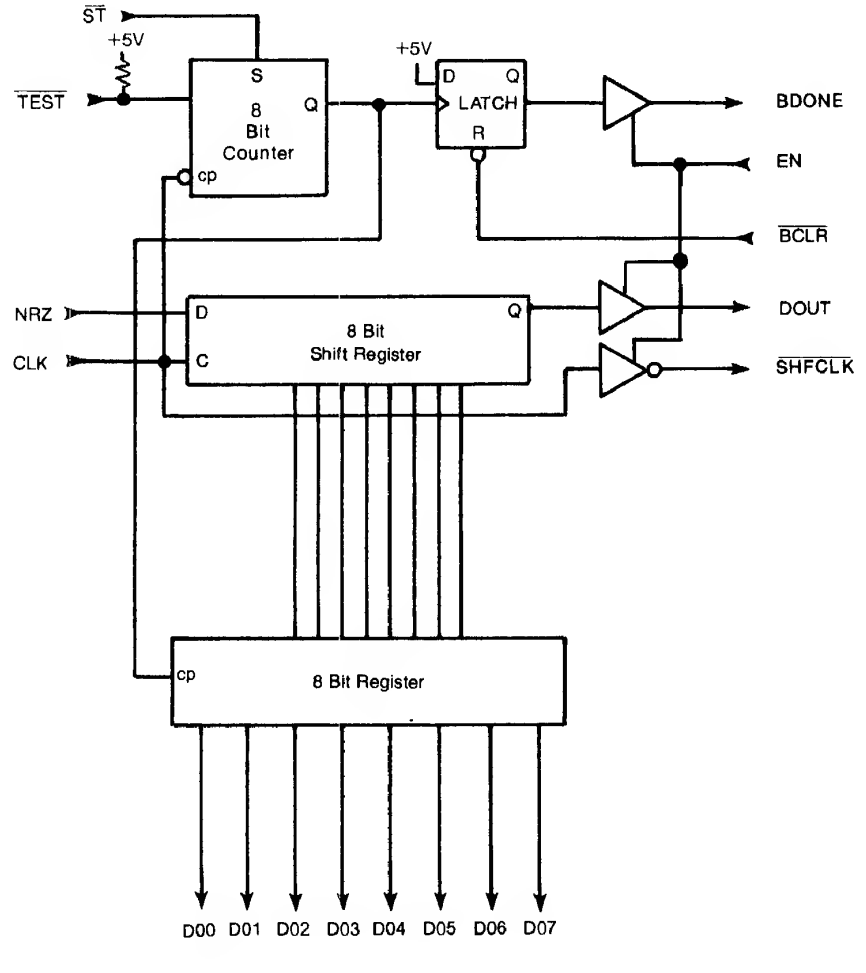
The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE



WD1100-01
Figure 1. Pin Connections



WD1100-01
Figure 2. Block Diagrams

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9, 11-13	D00-D07	DATA0-DATA7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. BCLR has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin
with respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation. . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC. . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

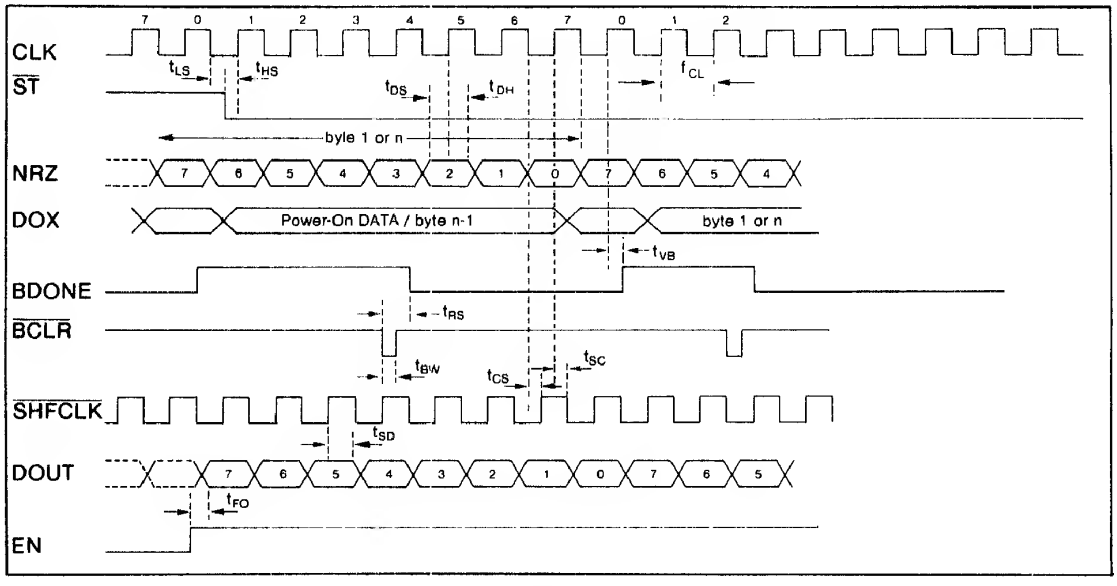
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑CLK	15			nsec	
t_{VB}	BDONE valid from ↑CLK	65		110	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			110	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑CLK to ↓$\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓CLK to ↑$\overline{SHFCLK}$			100	nsec	EN = 1
t_{SD}	Data delay from ↑$\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑CLK	25			nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-01
Figure 3.

See page 725 for ordering information.

Western Digital
WD1100-02 MFM Generator

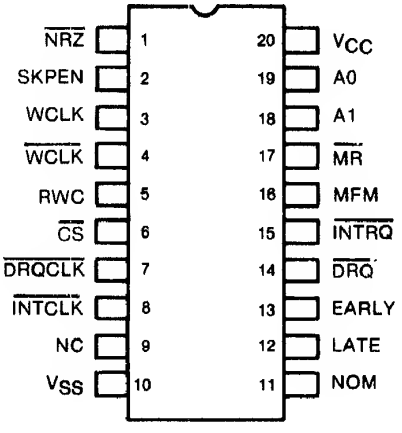
DESCRIPTION

The WD1100-02 MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-02 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

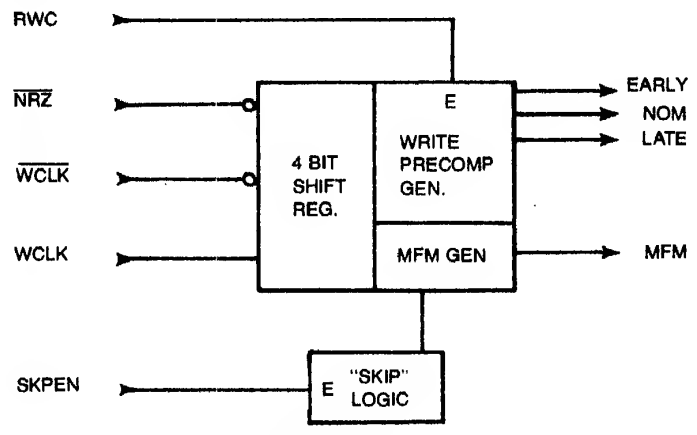
The WD1100-02 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

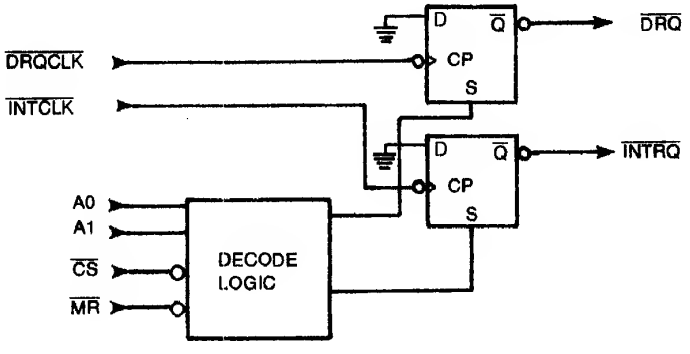
- SINGLE + 5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION
- 20 PIN DIP PACKAGE



WD1100-02
Figure 1. Pin Connections



WD1100-02
Figure 2. Block Diagram MFM Generator



WD1100-02
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	$\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$	NRZ data input that is strobed into the MFM generator by WCLK (↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	NC	No Connection	No Connection.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	$\overline{CHIP\ SELECT}$	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	$\overline{INTERRUPT\ REQUEST\ CLOCK}$	A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	$\overline{DATA\ REQUEST\ CLOCK}$	A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	$\overline{INTERRUPT\ REQUEST}$	This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled.
14	$\overline{DRQ}$	$\overline{DATA\ REQUEST}$	This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled.
17	$\overline{MR}$	$\overline{MASTER\ RESET}$	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 1, 0	When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ±10% power supply input.

DEVICE DESCRIPTION

The WD1100-02 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 8.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the $\overline{NRZ}$ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

$\overline{MR}$	A_1	A_0	$\overline{CS}$	$\overline{DRQ}$	$\overline{INTRQ}$
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only on the high-to-low transition of $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . −0.2V to + 7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE:
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C, V_{CC} = +5V ± 10%, V_{SS} = 0V

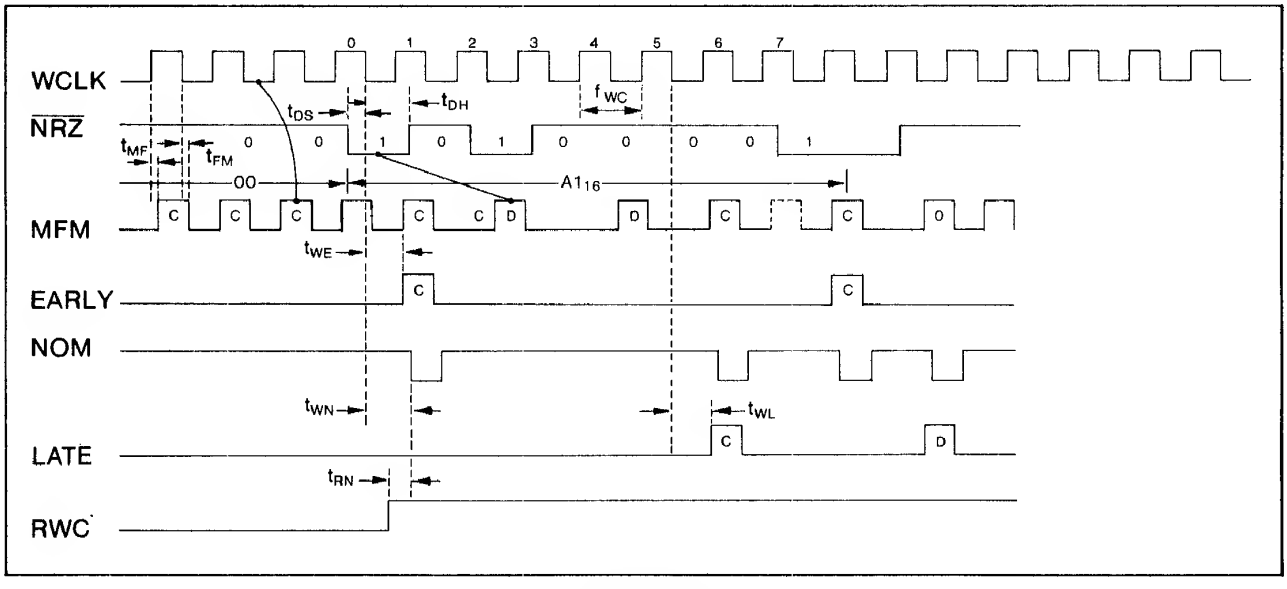
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{OC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

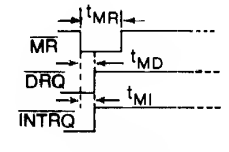
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓ WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓ WCLK	25			nsec	
t_{MF}	↑ WCLK to ↑ MFM delay			160	nsec	Pin 1 LOW
t_{FM}	↓ WCLK to ↓ MFM delay			180	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓ WCLK			190	nsec	Pin 4 = LOW
t_{WE}	Data delay to EARLY from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{WL}	Data delay to LATE from ↓ WCLK			180	nsec	Pin 4 = LOW
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓ $\overline{MR}$ to ↑ $\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑$\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓$\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓$\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑$\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑$\overline{INTRQ}$			160	nsec	
t_{CD}	↓$\overline{CS}$ to ↑$\overline{DRQ}$			145	nsec	
t_{CI}	↓$\overline{CS}$ to ↑$\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			115	nsec	

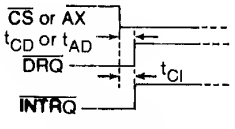
NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



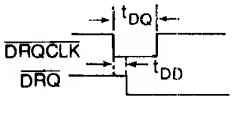
WD1100-02
Figure 4. MFM Generator Timing



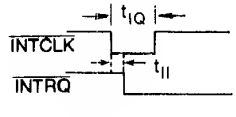
WD1100-02
Figure 5



WD1100-02
Figure 6



WD1100-02
Figure 7.



WD1100-02
Figure 8.

See page 725 for ordering information.

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PRELIMINARY

WD1100

Western Digital
WD1100-12 Improved MFM Generator

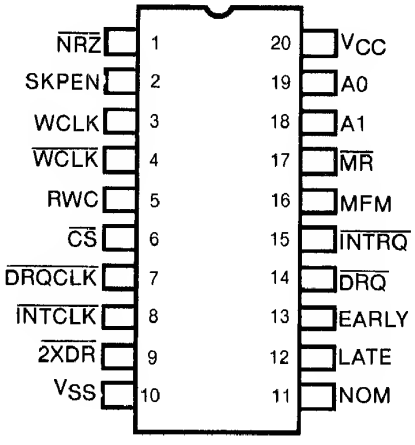
DESCRIPTION

The WD1100-12 improved MFM Generator converts NRZ data into an MFM (Modified Frequency Modulated) data stream. The derived MFM signal containing both clocks and data can then be used to record information on a Winchester Disk Drive utilizing this recording technique. In addition to an MFM output, the device generates first level Write Precompensation signals for use with inner track densities. A unique feature of the WD1100-12 is the ability to delete a clock pulse in the outgoing MFM stream in order to record Address Marks.

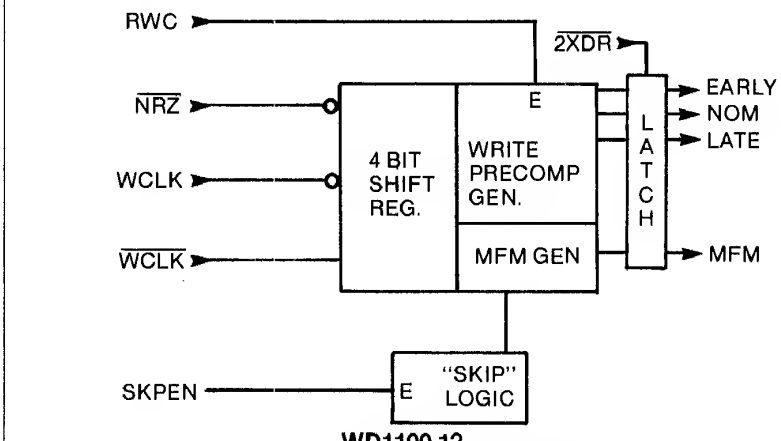
The WD1100-12 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

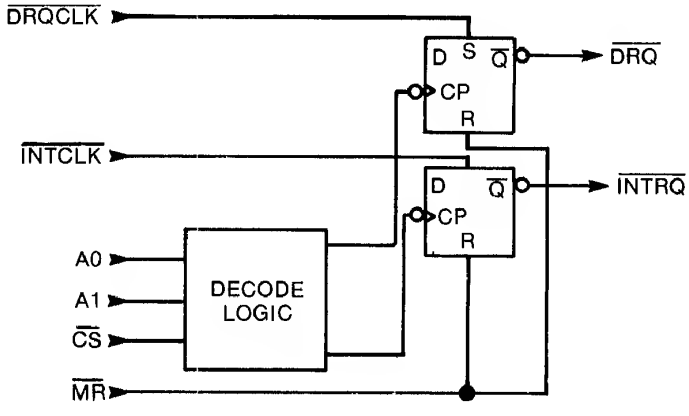
- SINGLE +5V SUPPLY
- 5 M BIT/SEC DATA RATE
- WRITE PRECOMPENSATION
- ADDRESS MARK GENERATION



WD1100-12
Figure 1. Pin Connections



WD1100-12
***Figure 2. Block Diagram MFM Generator**



WD1100-12
Figure 3. Block Diagram Interrupt Control Logic

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	$\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$	NRZ data input that is strobed into the MFM generator by WCLK(↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2XDR}$	$\overline{2\ TIMES\ DATA\ RATE}$	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	$\overline{CHIP\ SELECT}$	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	$\overline{INTERRUPT\ REQUEST\ CLOCK}$	A low on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	$\overline{DATA\ REQUEST\ CLOCK}$	A low on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	$\overline{INTERRUPT\ REQUEST}$	This output is latched at a logic 0 when INTCLK (pin 8) goes/ is low.
14	$\overline{DRQ}$	$\overline{DATA\ REQUEST}$	This output is latched at a logic 0 when DRQCLK (pin 7) goes/is low.
17	$\overline{MR}$	$\overline{MASTER\ RESET}$	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0,A_1	ADDRESS 0, 1	When CS is low and the address lines go high, INTRQ is cleared; if the address lines go low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

The WD1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic is used specifically on the WD1000 Winchester Controller Board and may be used in similar designs to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the $\overline{NRZ}$ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1. The algorithm used is on Page 4.

LAST DATA SENT		SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X	1	1	0	H	L	L
X	0	1	1	L	H	L
0	0	0	1	H	L	L
1	0	0	0	L	H	L
ANY OTHER PATTERN				L	L	H

DEVICE DESCRIPTION (CONTINUED)

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using $A1_{16}$ data with $0A_{16}$ clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the $A1_{16}$ the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used, the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests ($\overline{INTRQ}$) by selecting $\overline{CS}$ (pin 6) in combination with A_0 and A_1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INRQ}$ simultaneously.

MR	A_1	A_0	CS	DRQ	INTRQ
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care

Q_N = remains at previous state

$\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A_1, and A_0.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE:
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

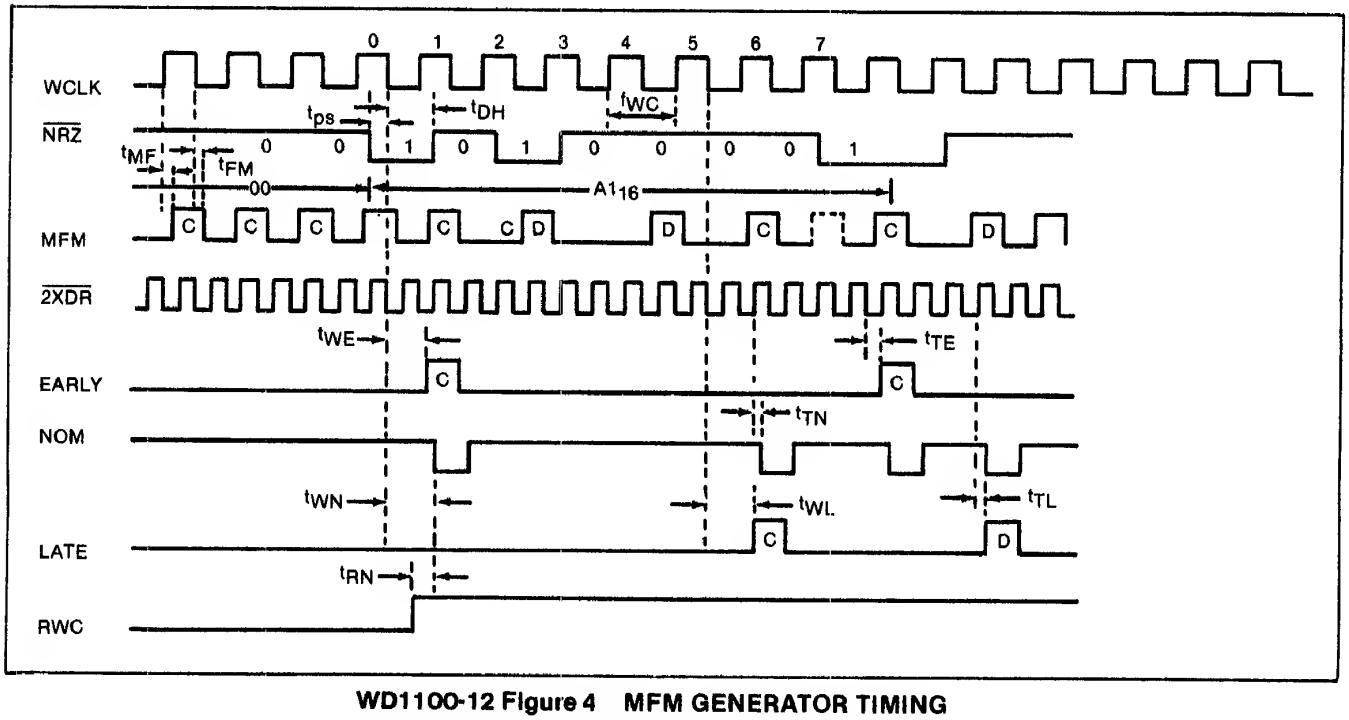
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

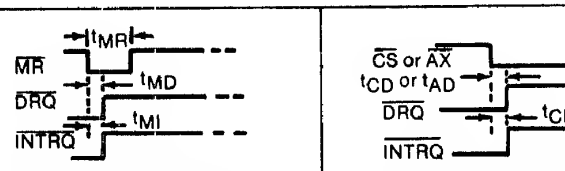
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓WCLK	25			nsec	
t_{MF}	↑WCLK to ↑MFM delay			210	nsec	Pin 1 LOW
t_{FM}	↓WCLK to ↓MFM delay			230	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓WCLK			240	nsec	
t_{WE}	Data delay to EARLY from ↓WCLK			230	nsec	
t_{WL}	Data delay to LATE from ↓WCLK			230	nsec	
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓$\overline{MR}$ to ↑$\overline{DRQ}$			150	nsec	

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{MI}	↓MR to ↑ $\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓ $\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓ $\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓AX to ↑ $\overline{DRQ}$			145	nsec	
t_{AI}	↑AX to ↑ $\overline{INTRQ}$			160	nsec	
t_{CD}	↓ $\overline{CS}$ to ↑ $\overline{DRQ}$			145	nsec	
t_{CI}	↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$			180	nsec	
t_{RN}	↑RWC to ↓NOM			145	nsec	
t_{TE}	↓ $\overline{2XDR}$ to ↑EARLY			75	nsec	
t_{TN}	↓ $\overline{2XDR}$ to ↑NOM			75	nsec	
t_{TL}	↓ $\overline{2XDR}$ to ↑LATE			75	nsec	

NOTES: 1. Typical Values are for $T_A = 25°C$ and $V_{CC} = +5.0V$.

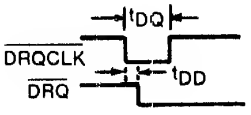


WD1100-12 Figure 4 MFM GENERATOR TIMING

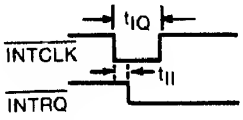


WD1100-12 Figure 5

WD1100-12 Figure 6



WD1100-12 Figure 7



WD1100-12 Figure 8

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-03 AM Detector

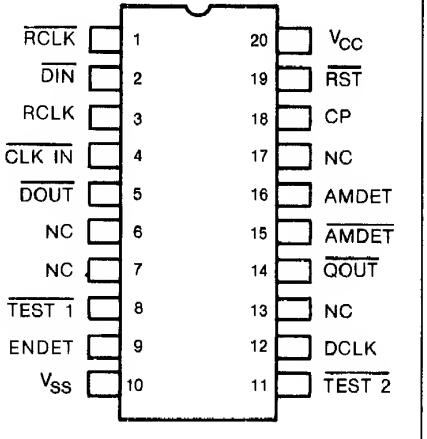
DESCRIPTION

The WD1100-03 Address Mark Detector provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM (NRZ) clocks and data are fed to the device along with a window clock generated by an external data separator. The WD1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces an AM DET signal when the pattern has been found. NRZ data is an output from the device, which can be used to drive a serial/parallel converter. An uncommitted latch is also provided for by the data separator circuitry, if required.

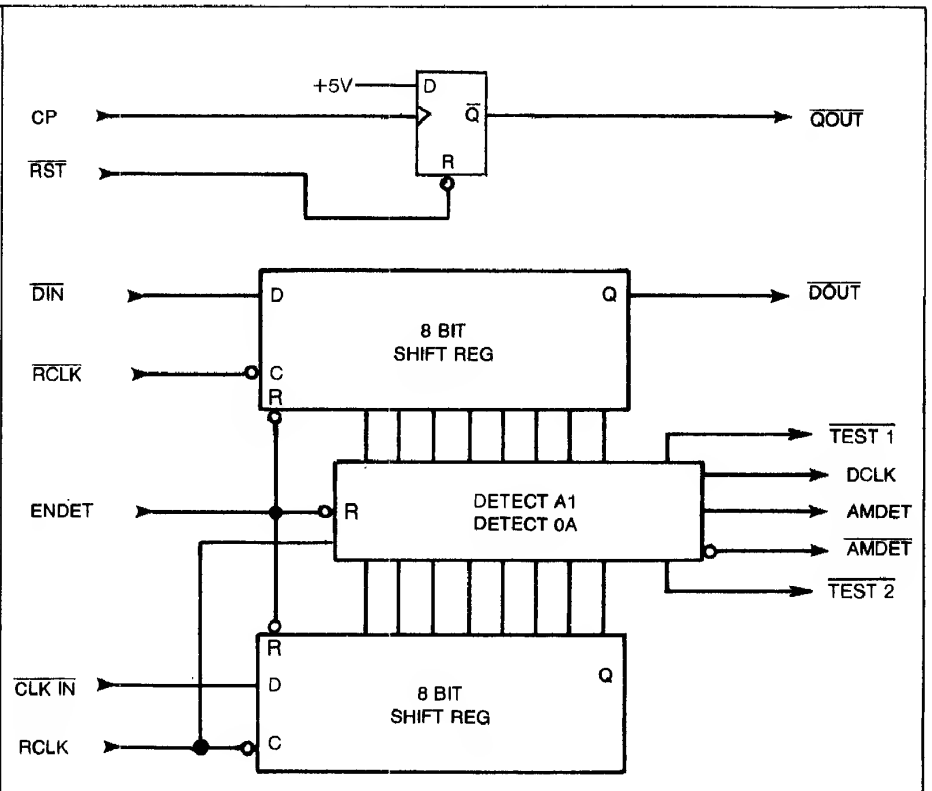
The WD1100-03 Address Mark Detector is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- 5 MBITS/SEC DATA RATE
- DECODES $A1_{16}$-$0A_{16}$
- SYNCHRONOUS CLOCK/DATA OUTPUTS
- 20 PIN DIP PACKAGE



WD1100-03
Figure 1. Pin Connections



WD1100-03
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1 3	$\overline{\text{RCLK}}$ RCLK	$\overline{\text{READ CLOCK}}$ READ CLOCK	Complimentary clock inputs used to clock DIN and $\overline{\text{CLK}}$ IN into the AM detector.
2	$\overline{\text{DIN}}$	$\overline{\text{DATA INPUT}}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{\text{CLK IN}}$	$\overline{\text{CLOCK INPUT}}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{\text{DOUT}}$	$\overline{\text{DATA OUTPUT}}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user
8 11	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{\text{DATA OUT}}$ (Pin 5).
14	$\overline{\text{QOUT}}$	$\overline{\text{LATCH OUTPUT}}$	Signal output from the uncommitted latch.
15	$\overline{\text{AMDET}}$	$\overline{\text{ADDRESS MARK DETECT}}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{\text{QOUT}}$ (Pin 14) to be latched at a logic 0.
19	$\overline{\text{RST}}$	$\overline{\text{RESET}}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and $\overline{\text{AMDET}}$, AMDET, $\overline{\text{CLK}}$, and $\overline{\text{DATA OUT}}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{\text{DIN}}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{\text{RCLK}}$ (Pin 1). NRZ clocks are entered on the $\overline{\text{CLK}}$ IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{\text{DOUT}}$ line (Pin 5) is tied to the last stage of the internal Data Shift register and will reflect information clocked into the DIN line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$, CLK = $0A_{16}$ pattern. When this pattern is detected, AMDET will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{\text{AMDET}}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{\text{DOUT}}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{\text{QOUT}}$ (Pin 14) to a logic 0. $\overline{\text{QOUT}}$ may be reset back to a logic 1 by a low level on the $\overline{\text{RST}}$ line (Pin 19).

$\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$ are output lines. $\overline{\text{TEST1}}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{\text{TEST2}}$ is active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias . . . . . 0°C to 50°C
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

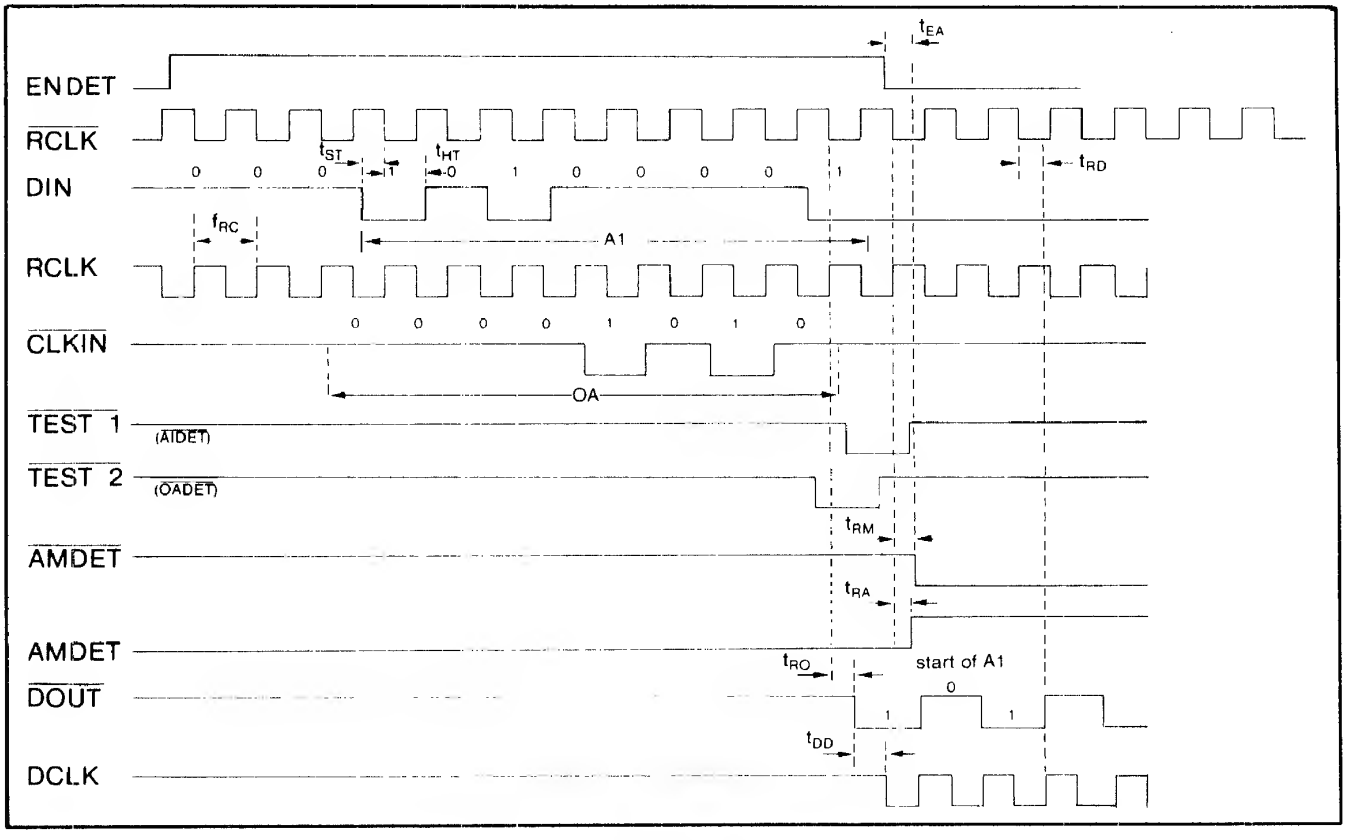
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓$\overline{RCLK}$ to ↑ DCLK			120	nsec	
t_{RA}	↓$\overline{RCLK}$ to ↑ AMDET			115	nsec	
t_{RM}	↓$\overline{RCLK}$ to ↓ $\overline{AMDET}$			125	nsec	
t_{RO}	↓$\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ENDET to ↓AMDET			130	nsec	
t_{RQ}	↓$\overline{RST}$ to ↑ $\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	↑CP to ↓ $\overline{QOUT}$			106	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5V.



WD1100-03
Figure 3. Functional Timing

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-04 CRC Generator/Checker

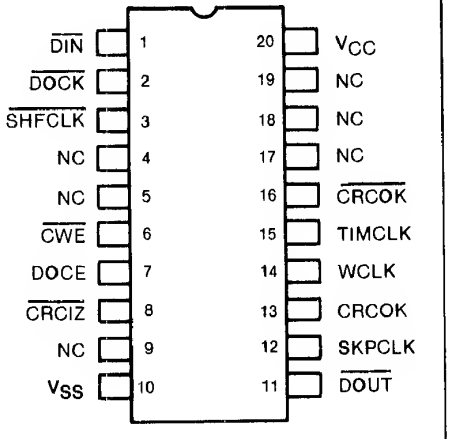
DESCRIPTION

The WD1100-04 CRC Generator/Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

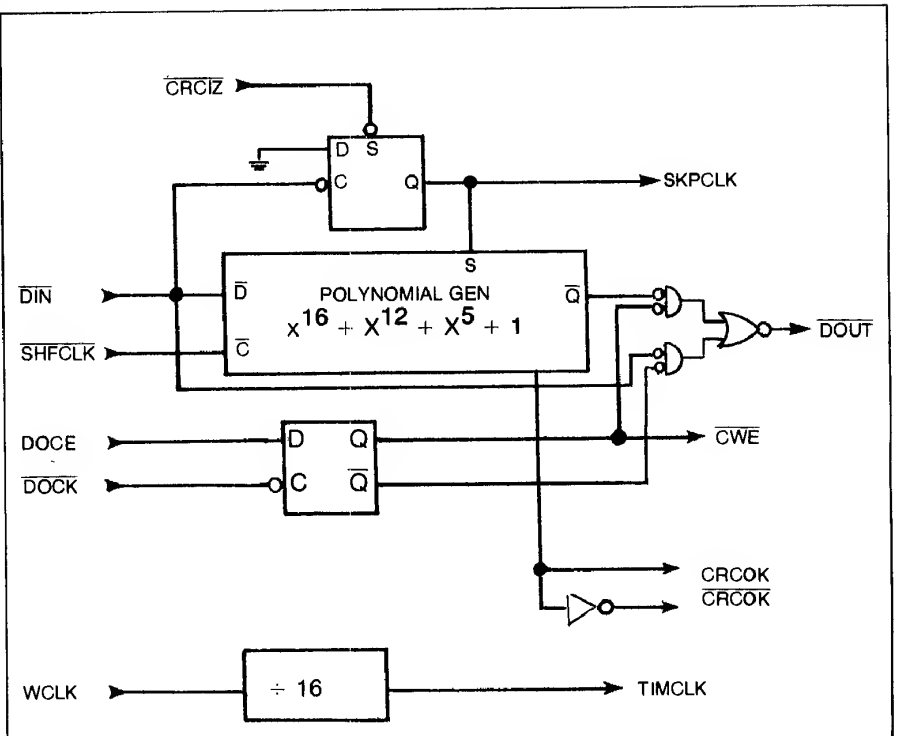
The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES/CHECKS CRC
- SINGLE +5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5 + 1$ (CCITT-16)
- AUTOMATIC PRESET
- 20 PIN DIP PACKAGE



WD1100-04
Figure 1. Pin Connections



WD1100-04
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4, 5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodifled data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See above.
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	V_{CC}	+5V ± 10% power supply input.

DEVICE DESCRIPTION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo $\overline{DOCK}$ is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line $\overline{DOUT}$ (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on $\overline{DIN}$ (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as $\overline{DIN}$ is held high and $\overline{CRCIZ}$ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°c to 50°c
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . −55°C to +125°C
CERAMIC . . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

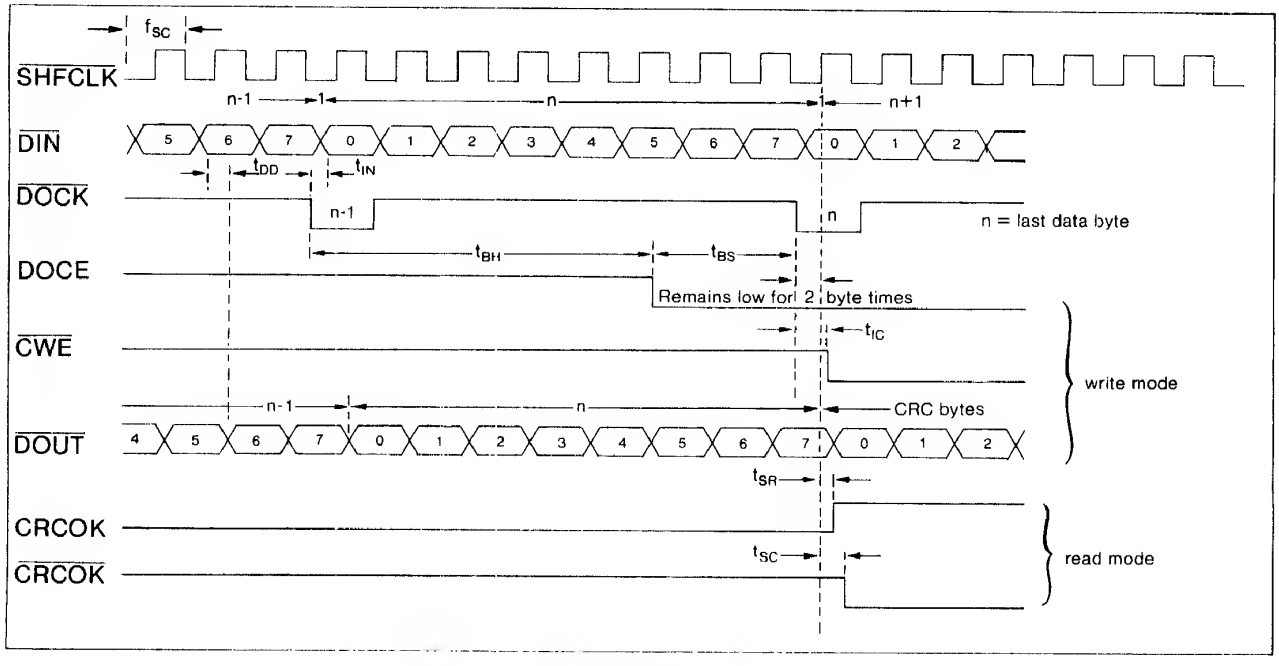
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0° to 50°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

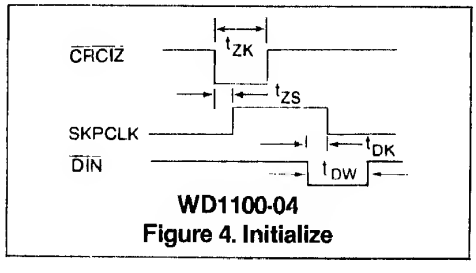
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WT}	↑WCLK to ↓TIMCLK			95	nsec	
t_{WR}	↑WCLK to ↑TIMCLK			85	nsec	
t_{ZS}	↓$\overline{CRCIZ}$ to ↑SKPCLK			120	nsec	
t_{ZK}	$\overline{CRCIZ}$ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓$\overline{DOCK}$	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓$\overline{DOCK}$	40			nsec	
t_{DD}	$\overline{DIN}$ to $\overline{DOUT}$ delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DK}	↓$\overline{DIN}$ to ↓SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{DOCK}$ to ↓ $\overline{CWE}$			120	nsec	
t_{BC}	↓ $\overline{DOCK}$ to ↑ $\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHZ	
t_{SR}	↑ $\overline{SHFCLK}$ to ↑ CRCOK			85	nsec	
t_{SC}	↑ $\overline{SHFCLK}$ to ↓ $\overline{CRCOK}$			90	nsec	
t_{IN}	↓ $\overline{DOCK}$ to ↓ $\overline{DIN}$			90	nsec	

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-04
Figure 3. Write Mode



WD1100-04
Figure 4. Initialize

See page 725 for ordering information.

Printed in U.S.A.

Western Digital
WD1100-05 Parallel/Serial Converter

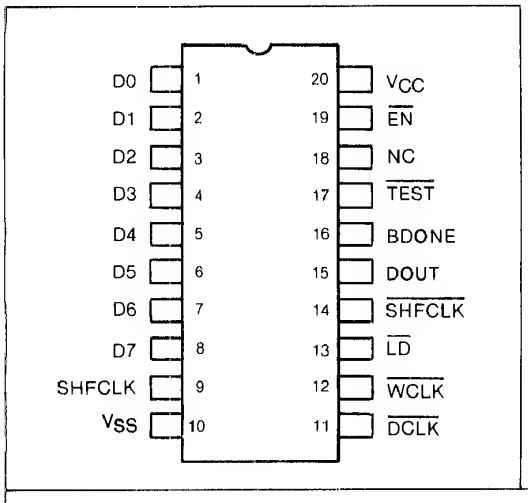
DESCRIPTION

The WD 1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

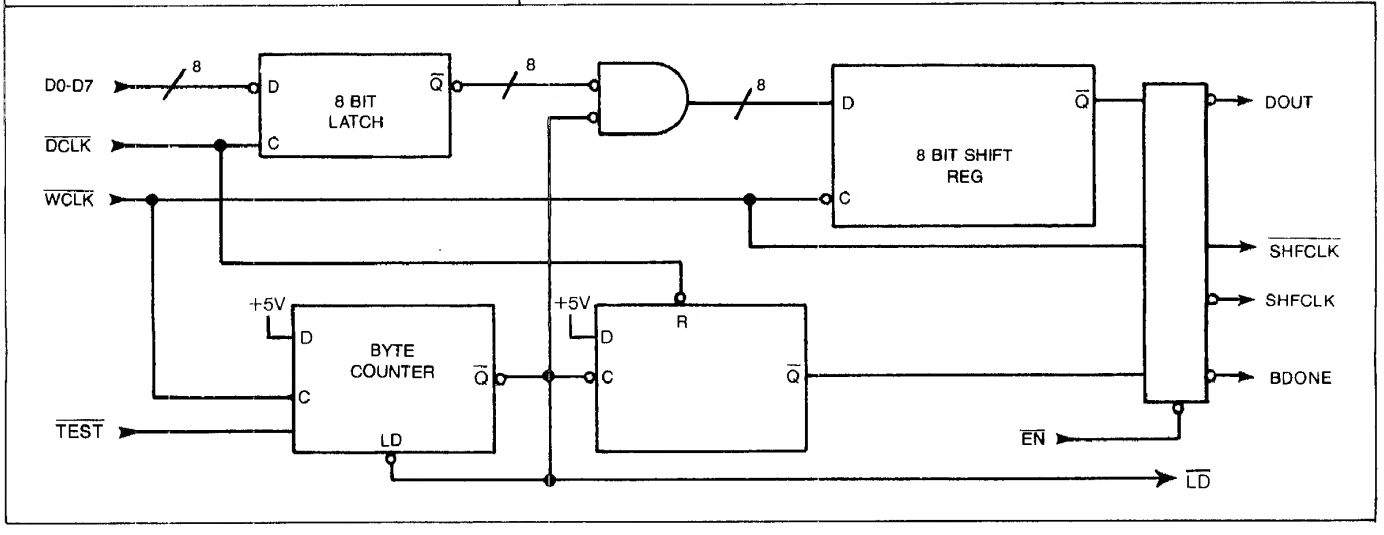
The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE + 5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE



WD1100-05
Figure 1. Pin Connections



WD1100-05
Figure 2. Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high (↑) transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 $\overline{\text{WCLK}}$ cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with respect to V_{SS} . . . −0.2V to +7.0V
Power Dissipation. . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC. . . . . −55°C to +125°C
CERAMICS. . . . . −55°C to +150°C

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

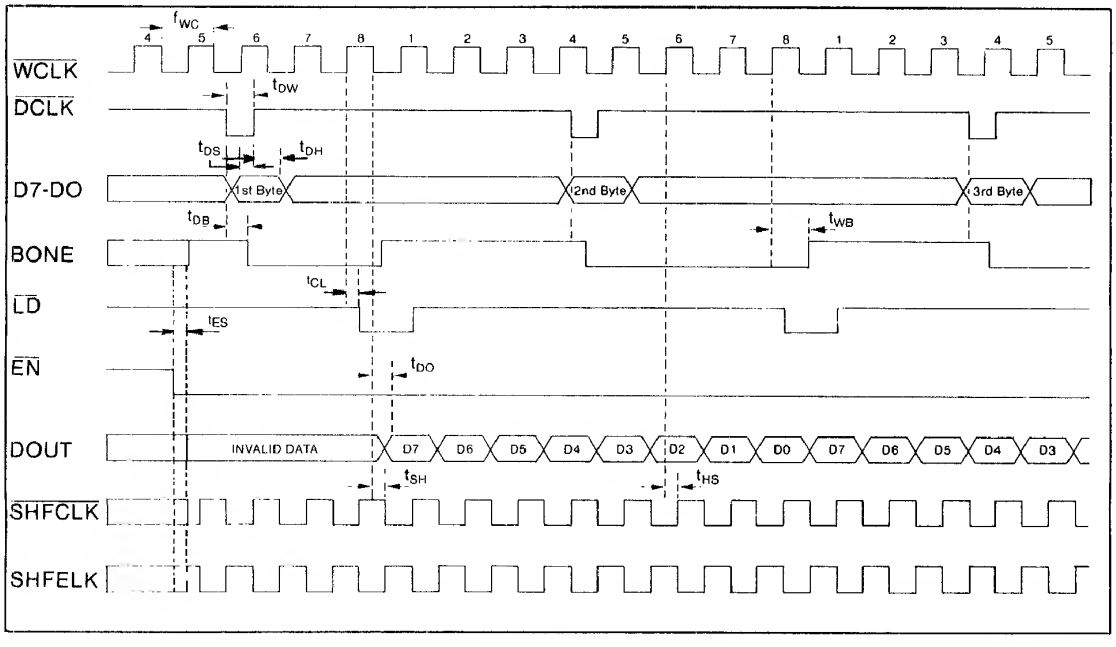
DC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC Electrical Characteristics: T_A = 0°C to 50°C; V_{CC} = +5 ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑ BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



WD1100-05
Figure 3. Functional Timing Diagram

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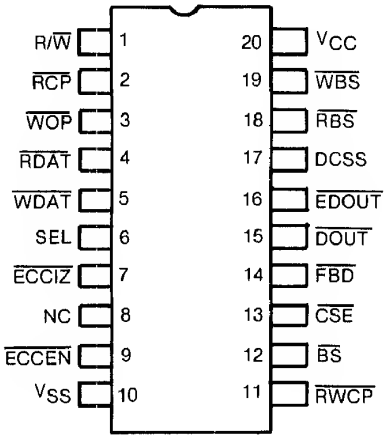
Western Digital
WD1100-06 ECC/CRC Logic

DESCRIPTION

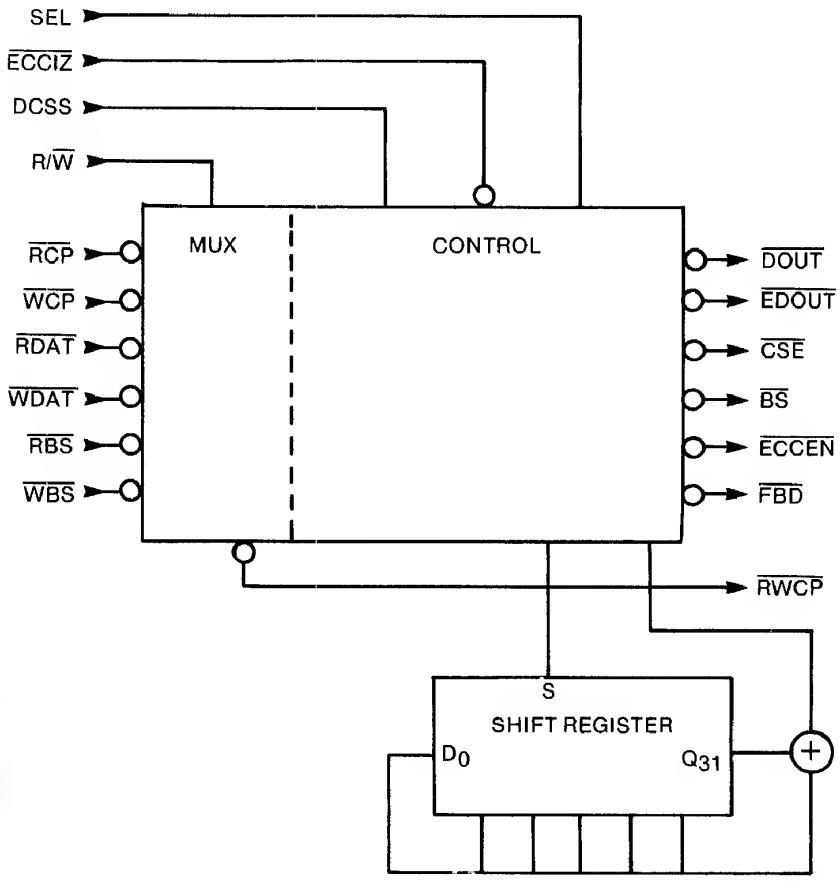
The WD1100-06 ECC/CRC logic chip gives the user of the WD1100 series of chips easy ECC or CRC implementation. With proper software, it will provide single burst correction up to 8 bits and double burst detection. The computer selected polynomial has been optimized for Winchester 5¼" and 8" drives with sector sizes up to 512 bytes.

FEATURES

- 32 bit computer selected polynomial
- Single burst correction up to 8 bits
- Multiple burst detection
- Programmable correction/detection span
- CRC or ECC software selectable
- Data transfer rates to 5.25 Mbits/sec
- Serial check/syndrome bit processing
- 128, 256, 512 byte sector sizes
- Single +5V supply
- TTL, MOS compatible
- 20 pin DIP package



WD1100-06 Figure 1.
PIN CONNECTIONS



WD1100-06 Figure 2.
BLOCK DIAGRAM

WD1100-06 ECC/CRC DEVICE PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ/WRITE	R/W	Input line used to select the data, clock and CRC/ECC strobe during read/write operations. When low input signals WDAT, WCP, and WBS are selected. When high input signals RDAT, RCP, and RBS are selected.
2	READ CLOCK PULSE	RCP	Input pulse used by the internal shift registers to compute the 4 syndrome bytes.
3	WRITE CLOCK PULSE	WCP	Input pulse used by the internal shift registers to compute the 4 check bytes.
4	READ DATA	RDAT	Serial data input during a read operation.
5	WRITE DATA	WDAT	Serial data input during a write operation.
6	SELECT	SEL	This input is used to select either the CRC or the ECC polynomial for error detection/correction. SEL = 0 ECC polynomial selected. SEL = 1 CRC polynomial selected.
7	ECC INITIALIZE	ECCIZ	Input used to preset all the internal shift registers. Output lines FBD, EDOUT, DOUT, and CSE will be in their inactive high states. The first low going edge of either RDAT or WDAT signals the activation of all internal circuitry.
8	NO CONNECTION	N/C	No connection.
9	ECC ENABLE	ECCEN	When low, the ECC/CRC process is enabled. When high, this output signal indicates that the process is disabled.
10	GROUND	V_{SS}	Ground
11	READ/WRITE CLOCK PULSE	RWCP	Output clock pulse during read or write operations. The input clock pulses RCP and WCP are multiplexed on this output line for use by any support logic.
12	BYTE SYNC	BS	The input signals RBS and WBS are gated with the appropriate clocks and multiplexed as an output on the byte sync line. Normally not used by the user.
13	CLOCK SELECT ENABLE	CSE	When high, this output indicates that the device is in the process of computing the check/syndrome bytes and that EDOUT and DOUT lines contain data information. When low, the device puts CRC or ECC check/syndrome bits on the output data lines.
14	FEEDBACK	FBD	The feedback line to the shift registers is brought out as an output line for test purposes. Normally left open by the user.
15	DATA OUTPUT	DOUT	Output data line carries data or CRC/ECC information depending upon the state of DCSS.
16	EARLY DATA OUTPUT	EDOUT	Unlatched output data line available 1 clock period earlier than DOUT.

WD1100-06 ECC/CRC PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	DATA/CHECK SYNDROME SELECT	DCSS	Data or check/syndrome select input line. When high, data is output on the data lines; when low, CRC or check syndrome bits are output depending upon which polynomial is selected. DCSS goes low sometime between the last and the next to the last data byte transferred to/from the disk provided all set-up and hold-times have been met. DCSS must stay low for at least 2 byte times when the CRC polynomial selected and it must stay low for at least 4 byte times if the ECC polynomial is selected.
18	$\overline{\text{READ BYTE}}$	$\overline{\text{RBS}}$	Input used to latch the state of DCSS during the read mode.
19	$\overline{\text{WRITE BYTE}}$	$\overline{\text{WBS}}$	Input used to latch the state of DCSS during the write mode.
20	+5V	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

To ensure correct operation of the WD1100-06 device, the $\overline{\text{ECCIZ}}$ line is strobed to preset the polynomial generator shift register, and reset the Data/Check-Syndrome select flip-flop. The 32 bit shift register string is preset to avoid all zero check bytes. The DCSS line is held high and appropriate signals are then applied to the rest of the inputs. Since most disk media use an Address mark of A1 (or M.S.B. set), advantage is taken of this feature to start off the ECC/CRC calculation on the data/ID fields automatically. The first active low going edge on the input data lines releases the internal SET Flip-Flop. The $\overline{\text{ECCEN}}$ output line is set low indicating that the internal circuitry is ready to begin the computation of the ECC/CRC bytes. Immediately following the Address mark, data is supplied in a serial fashion.

Sometime before the last byte of data and after the next to the last byte of data is transferred through this device, the DCSS line is set low. Since data is generally serialized/deserialized before/after processing by the WD1100-06 device, the byte-sync pulses can be easily obtained from those devices marking the byte boundaries. The byte-sync pulses are internally ANDED with the $\overline{\text{RWCP}}$ line to ensure the smooth transition of check/syndrome bytes on the $\overline{\text{DOUT}}$ output line only after the last bit of data has been entered into the device. A one bit time delay through a D Flip-Flop has been added on the $\overline{\text{DOUT}}$ line to deglitch this output line.

During a WRITE operation, the input data stream is divided by the polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^2 + 1$ and the 32 bit remainder obtained is used as the 4 check syndrome bytes. If the syndrome is zero, no errors occurred. Otherwise, the non-zero syndrome is used by a software algorithm to compute the displacement and the error vector within the bad sector. To protect the integrity of the ID field only a CRC check should be performed over this field. No attempt ought to be made to correct data in the ID field. The CRC polynomial implemented is the standard CCITT ($X^{16} + X^{12} + X^5 + 1$.) Although either polynomial may be used for both fields, the use of the CRC polynomial for the ID fields is recommended since it only requires 2 bytes instead of 4.

POLYNOMIAL SELECTION

For disk media, polynomial selection has a significant influence on data accuracy. Fire code polynomials have been widely used on OEM disk controllers, but provide less accuracy than properly selected computer generated codes.

For fixed, guaranteed correction and detection spans, data accuracy may be highly dependent on polynomial selection. Some polynomials, fire codes for example, are particularly susceptible to miscorrection on common disk type errors, while others, computer generated polynomials for example, can be selected to be less susceptible. Computer generated codes do not have the pattern sensitivity of the fire code and the miscorrection patterns are more random in nature.

More than 20,000 computer generated random polynomials of degree 32, each with 8 feedback terms, were evaluated in order to find the polynomial described in this specification.

SELECTING THE CORRECTION SPAN

The code described in this document can be used to correct up to 8 bits.

Any correction span from 1 to 8 may be selected. However, for best data accuracy, the lowest correction span should be used that meets the correction

requirements for the disk drives supported.

For most Winchester media, a 5 bit correction span is adequate.

The correction span may have to be longer if the drive uses a read/write modulation method that maps a single media bit in error into several decoded bits in error. Examples of read/write modulation methods of this type would be GCR and 2,7 code.

PROPERTIES OF THE POLYNOMIAL

The following polynomial was computer selected for insensitivity to short double bursts, good detection span and 8 feedback terms.

Forward polynomial is:
$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 0$

Reciprocal polynomial is:
$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + x^{13} + X^6 + X^4 + X^0$

Properties*

1. Maximum record length (r) = 526x8 bits (including check bits)
2. Maximum correction span (b) = 8 bits
3. Degree of polynomial (m) = 32
4. Single burst detection span without correction = 32 bits. (Detection span when the code is used for detection only)
5. Single burst detection span with correction (d) — (Detection span when the code is used for correction)
   - = 19 bits for b = 5 and r = 526x8
   - = 14 bits for b = 8 and r = 526x8
   - = 20 bits for b = 5 and r = 270x8
   - = 14 bits for b = 8 and r + 270x8
6. Double burst detection span without correction — (Doule burst detection span when code is used for correction)
   - = 3 bits for b = 5 and r = 526x8
   - = 2 bits for b = 8 and r = 526x8
   - = 4 bits for b = 5 and r = 270x8
   - = 2 bits for b = 8 and r = 270x8
7. Non-detection probability = 2.3 E-10.
8. Miscorrection probability—
   - = 1.57 E-5 for b = 5 and r = 526x8
   - = 1.25 E-4 for b = 8 and r = 526x8
   - = 8.00 E-6 for b = 5 and r = 270x8
   - = 6.40 E-5 for b = 8 and r = 270x8

NOTE:*
You should not use this polynomial for a record length or correction span beyond the maximum specified above.

SOFTWARE REQUIREMENTS

The software algorithm, developed by the user, uses the syndrome to detect an error, generate a correction pattern and a displacement vector or to determine if uncorrectable. In the correction algorithm, a simulated shift register is used to implement the reciprocal polynomial. The simulated shift register is loaded with the syndrome and shifted until a correctable pattern is found or the error is determined to be uncorrectable. Both forward and reverse displacements are computed.

Either the serial or the parallel algorithm may be implemented by the user. In almost all cases the serial software algorithm is the most applicable. Additionally, 1K of table space is required if the parallel software algorithm is selected. It is assumed that the highest order bit of a byte is serialized and deserialized first.

CORRECTION TIME PERFORMANCE

All real time operations are performed with error correction hardware. The software algorithms used get involved only after an error has been detected.

The following correction times are for a serial type algorithm such as that used on the WD1001:

a) Standard microprocessor = 30 to 60 milliseconds
b) Bit slice = 6 to 12 milliseconds
c) 8X300 (used on WD1001) = 15 to 30 milliseconds

DATA ACCURACY

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be re-read before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected erroneous data by rereading until the error goes away, or until there has been a consistant error syndrome over two previous rereads.

Another technique that can be used to give data a higher probability of recovery is write check: read back after write. Since write check affects performance, it should be optional. Alternate sector assignment and defect skipping are some of the other techniques that may be implemented by the user if so desired.

SELF-CHECKING WITH MICROCODE

Periodic microcode and/or software checking is another approach that can be used to limit the amount of undetected erroneous data transferred in case of an ECC circuit failure. Microcode or software diagnostics could be run on subsystem power up and during idle times. These diagnostics would force ECC errors and check for the proper syndrome and proper decoding of the syndrome by the correction routine of the operational microcode.

To do this, simply use a long bit in the READ and WRITE commands to the disk. This bit can then be used to suppress the transfer of check/syndrome bytes on the output data line by letting the DCSS line stay high during ECC TIME. The complete procedure is summarized below.

1. WRITE: Pass all data to the disk and generate 4 check bytes at the end of the data field.
2. READLONG: Do not generate the syndrome, instead copy the 4 check bytes as data and pass them unaltered to the host. Now the host may induce errors anywhere in the data stream as long as the induced error does not exceed the correction span of the polynomial generator.
3. WRITELONG: Write the data and check bytes supplied by the host to the disk. Prevent WD1100-06 from generating check bits by not asserting DCSS during transfer. No check bytes will be recorded.
4. READ: Read data and generate the syndrome in a normal manner. The software algorithm can now be invoked to correct the induced error.

To aid in detection of certain hardware failures, it is desirable to have non-zero check bytes for an all zeros record. This feature has been incorporated into the circuit defined in this specification.

SPECIFICATIONS

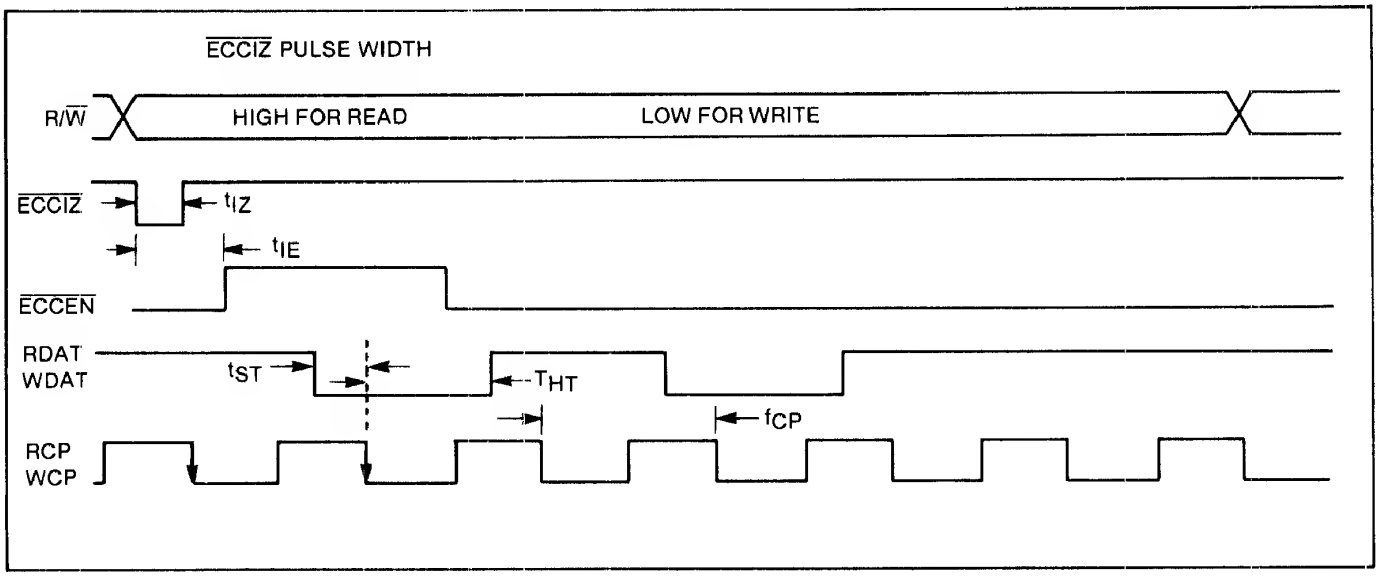
ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2V to +7.0V
Power dissipation . . . . . 1 Watt
Storage Temperature
Plastic . . . . . −55°C to +125°C
Ceramic . . . . . −55°C to +150°C

NOTE:
Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		75	150	mA	All outputs open



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS}

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{CP}	Clock Frequency			5.25	MHZ	
t_{IZ}	$\overline{ECCIZ}$ Pulse Width	50			nSec	
t_{IE}	$\overline{ECCIZ}$ ↓ to $\overline{ECCEN}$ ↑			100	nSec	
t_{ST}	R/WDAT Setup Time	50		1 Clock Period	nSec	
t_{HT}	R/WDAT Hold Time	0			nSec	

See page 725 for ordering information.

PRELIMINARY

WD1100-07

Western Digital
WD1100-07 Host Interface Logic

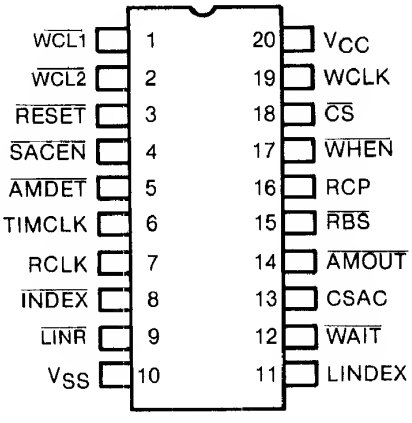
DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

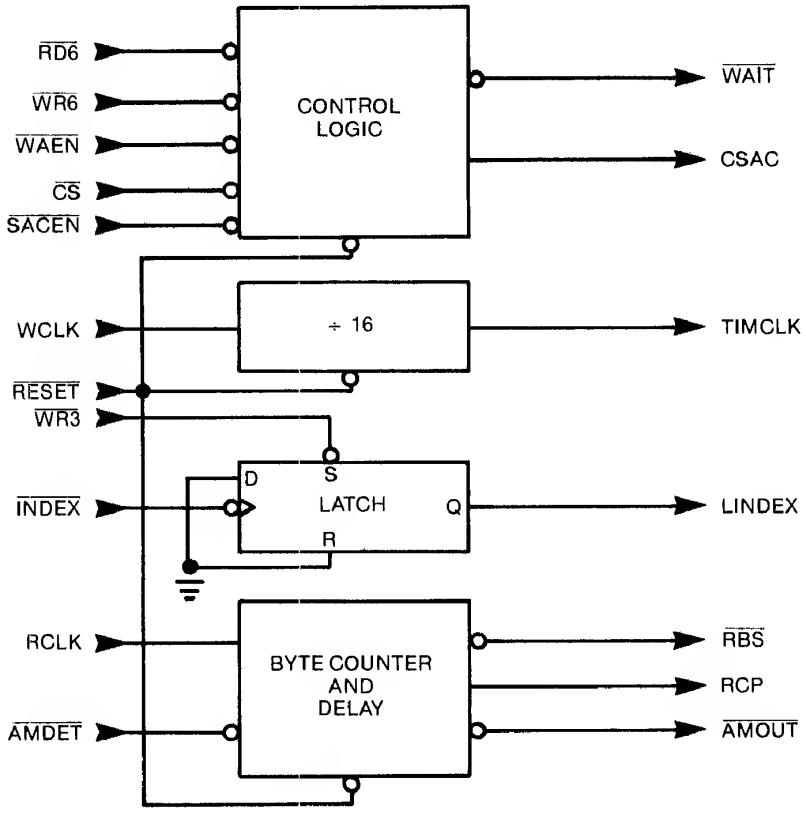
The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic Dual-in-Line package.

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE



WD1100-07 Figure 1.
PIN CONNECTIONS



WD1100-07 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	WCL1	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	WCL2	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	RESET	An input used to set TIMCLK & reset WAIT, AMOUT and RBS.
4	SELECT ADDRESS ENABLE	SACEN	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	AMDET	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce AMOUT.
8	INDEX PULSE	INDEX	This input is provided by the drive once each revolution of the disk
9	LINDEX RESET	LINR	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground
11	LATCHED INDEX	LINDEX	An output that is INDEX delayed by one clock time.
12	WAIT	WAIT	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of CS qualified with SACEN.
14	ADDRESS MARK DELAYED OUTPUT	AMOUT	This output is a delayed version of AMDET.
15	READ BYTE STROBE	RBS	This output strobes once for each byte of READ data. Initialized by AMDET.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	WAEN	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	CS	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%

DEVICE DESCRIPTION

Upon power up or reset, WAIT, AMOUT, and RBS are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides WAIT (pin 12) and CSAC (pin 13). WAIT is set in its active low state when WAEN (pin 17) is active low by the falling edge of CS (pin 18). WAIT is reset by the falling edge of either WCL1 or WCL2 depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting SACEN (pin 4) low after WAIT has been enabled. CSAC is reset by WCL1 or WCL2.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of INDEX (pin 8). It remains high until reset by LINR (pin 9).

Read Byte Sync

RBS (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after AMDET (pin 5) goes true. RBS will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

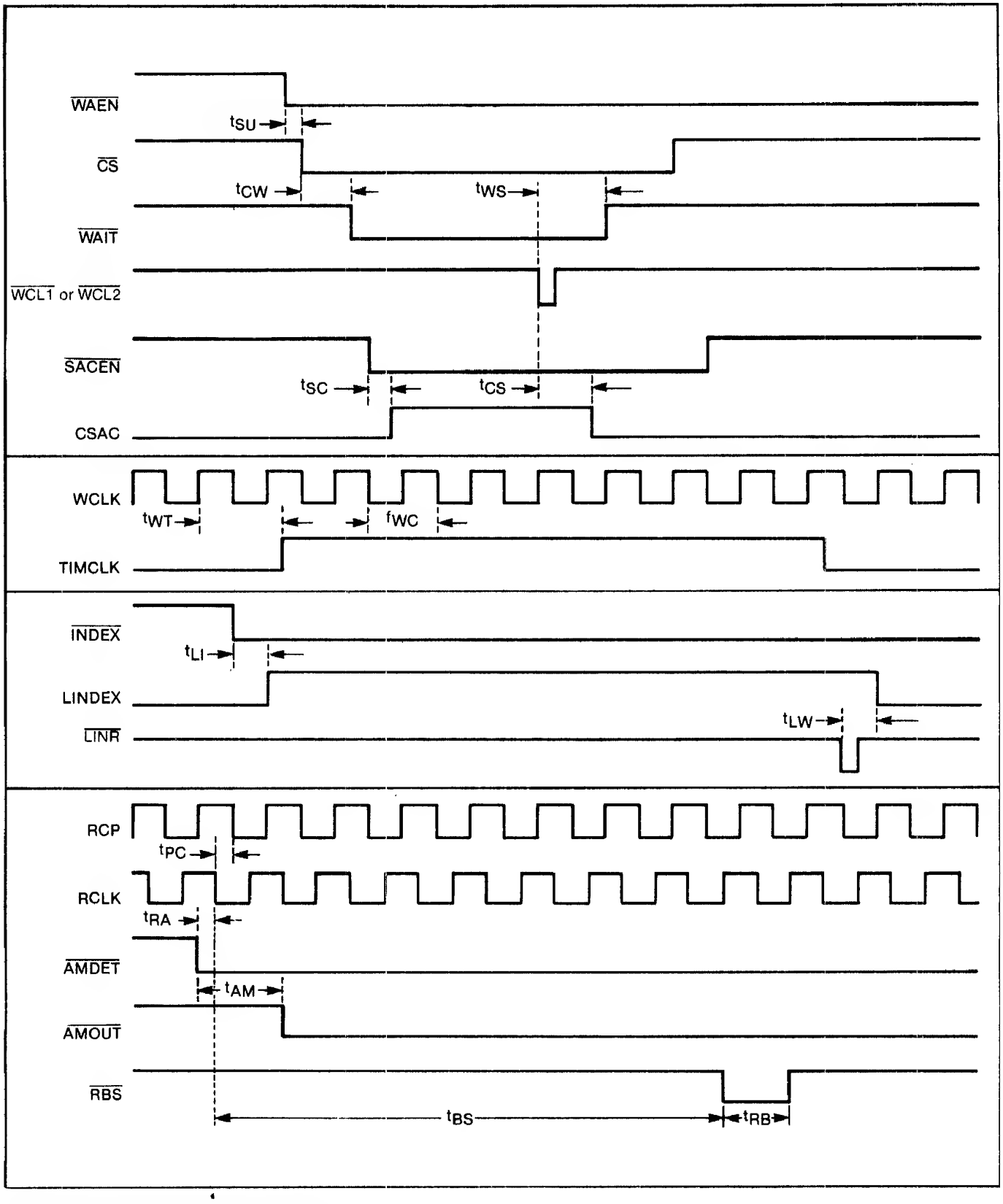
DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
f_{WC}	WCLK FREQUENCY			5.25	MHZ	
t_{CW}	CS↓ to WAIT↓		50	160	nSec	
t_{WS}	WCL1↓ or WCL2↓ to WAIT↑		170	195	nSec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nSec	
t_{SC}	SACEN↓ to CSAC↑		5	70	nSec	$\overline{WAIT}$ TRUE
t_{CS}	WCL1↓ or WCL2↓ to CSAC↓		45	155	nSec	$\overline{WAIT}$ TRUE
t_{WT}	WCLK↑ to TIMCLK↑			250	nSec	
t_{LI}	INDEX↓ to LINDEX↑		50	100	nSec	
t_{LW}	LINR↓ to LINDEX↓		30	100	nSec	
t_{PC}	RCLK↓ to RCP↓		30	75	nSec	
t_{RA}	AMDET Setup Time	30	50		nSec	
t_{AM}	AMDET↓ to AMOUT↓		2 CLOCK CYCLES	2 CLOCK CYCLES + 45	nSec	
t_{BS}	RCLK↓ to RBS↓		8 CLOCK CYCLES	8 CLOCK CYCLES + 165	nSec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1] NOTE: Typical Values are for T_A = 25°C and V_{CC} = +5V



See page 725 for ordering information.

PRELIMINARY

Western Digital
WD1100-09 Data Separator Support Logic

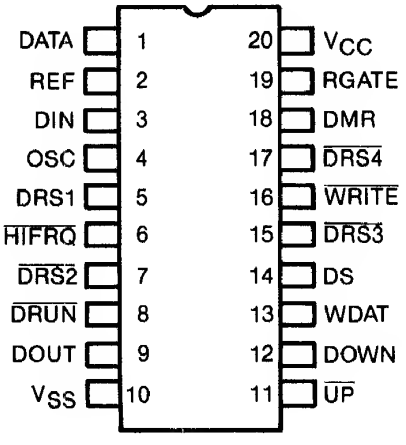
GENERAL DESCRIPTION

The WD1100-09 Data Separator Support Logic, when used with the other chips in the WD1100 series, greatly reduces the external discrete logic required to design a Winchester hard disk data separator. The chip provides the pump signals to an external error amplifier, control signals to an internal bus and a special drive selection signal also to an internal bus.

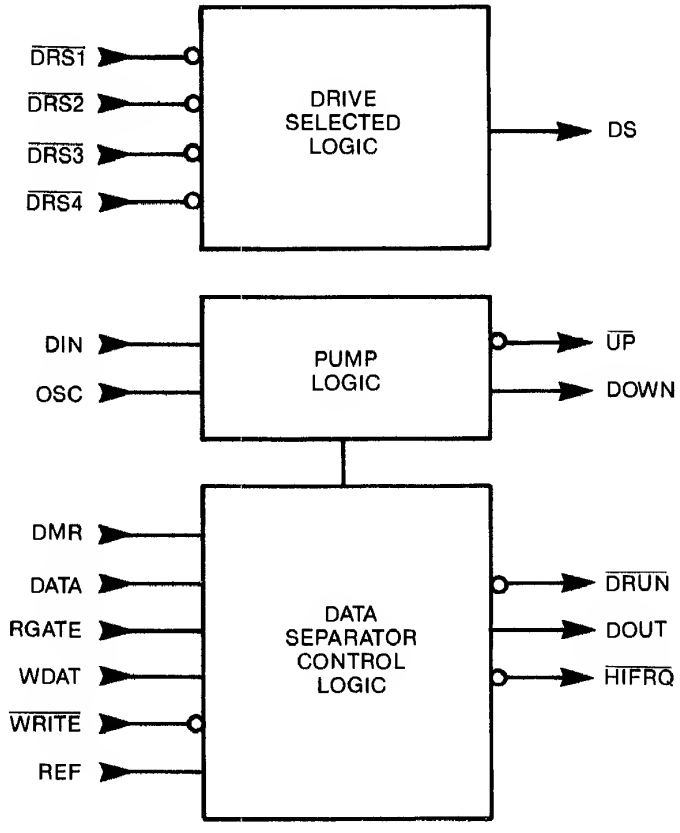
The WD1100-09 is fabricated in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic package.

FEATURES

- SINGLE +5V SUPPLY
- DRUN GENERATION
- DATA SEPARATION CONTROL SIGNALS
- 20 PIN DIP PACKAGE



WD1100-09 Figure 1.
PIN CONNECTIONS



WD1100-09 Figure 2.
BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	READ DATA	DATA	Input that is used in $\overline{\text{DRUN}}$ generation.
2	REFERENCE	REF	An input that is 2 times the data rate that keeps the VCO on center frequency during non-read times.
3	DELAYED DATA IN	DIN	This input is a delayed version of DOUT. An external delay line is used. The signals are compared to provide pumps.
4	OSCILLATOR	OSC	An input from the external VCO that is used in pump development
5, 7, 15, 17	$\overline{\text{DRIVE SELECT}}$ 1- $\overline{\text{DRIVE SELECT}}$ 4	$\overline{\text{DRS1}}$- $\overline{\text{DRS4}}$	Input signals indicating which drive has been selected.
6	$\overline{\text{HIGH FREQUENCY}}$	$\overline{\text{HIFRQ}}$	Output to controller microprocessor that indicates 16 ones or zeros have been entered on the DATA line.
8	$\overline{\text{DATA RUNNING}}$	$\overline{\text{DRUN}}$	Output that indicates to the controller microprocessor the completion of 16 ones or zeros on the data line. Used to switch from REF to DATA via firmware.
9	DATA OUT	DOUT	Output data line. Can be REF or $\overline{\text{DATA}}$ or $\overline{\text{WDATA}}$ depending on the condition of $\overline{\text{WRITE}}$, $\overline{\text{DMR}}$ and RGATE.
10	GROUND	V_{SS}	Ground
11	$\overline{\text{UP PUMP}}$	$\overline{\text{UP}}$	An output that indicates REF is leading DATA. Goes to error amp. Open collector.
12	DOWN PUMP	DOWN	An output that indicates DATA is leading REF. Goes to error amp. Open collector.
13	WRITE DATA	WDATA	MFM Write data input. Output appears at DOUT.
14	DRIVE SELECTED	DS	An output that indicates that one of four drives have been selected.
16	$\overline{\text{WRITE MODE}}$	$\overline{\text{WRITE}}$	This input is active during a write operation and enables WDAT.
18	DATA MASTER RESET	DMR	This input is used to provide time-out for $\overline{\text{DRUN}}$ and $\overline{\text{HIFRQ}}$ in the event that 16 ones or zeros are not present.
19	READ GATE	RGATE	This input, usually provided by the controller microprocessor, places chip in read mode.
20	+5VDC	V_{CC}	+5VDC ± 10%

DEVICE DESCRIPTION

The WD1100-09 is divided into three sections. Each section will be described separately.

Drive Select Logic

DS (pin 14) will go active high if any input $\overline{\text{DSR1}}$ through $\overline{\text{DRS4}}$ (pins 5, 7, 15, 17) are active low.

Pump Logic

Internal logic causes the $\overline{\text{UP}}$ (pin 11) and the DOWN (pin 12) to be set, initially to their inactive states. DIN (pin 3) is the delayed data developed by passing DOUT through a delay line. OSC (pin 4) is the output of the data separator VCO. Whichever reaches the pump logic first will determine whether UP PUMP or DOWN PUMP is produced. These signals are then sent to an external error amplifier and used for VCO correction. During a write, the DIN must be locked to a crystal oscillator clock and will hold the VCO on frequency.

Data Separator Control Logic

Read Mode

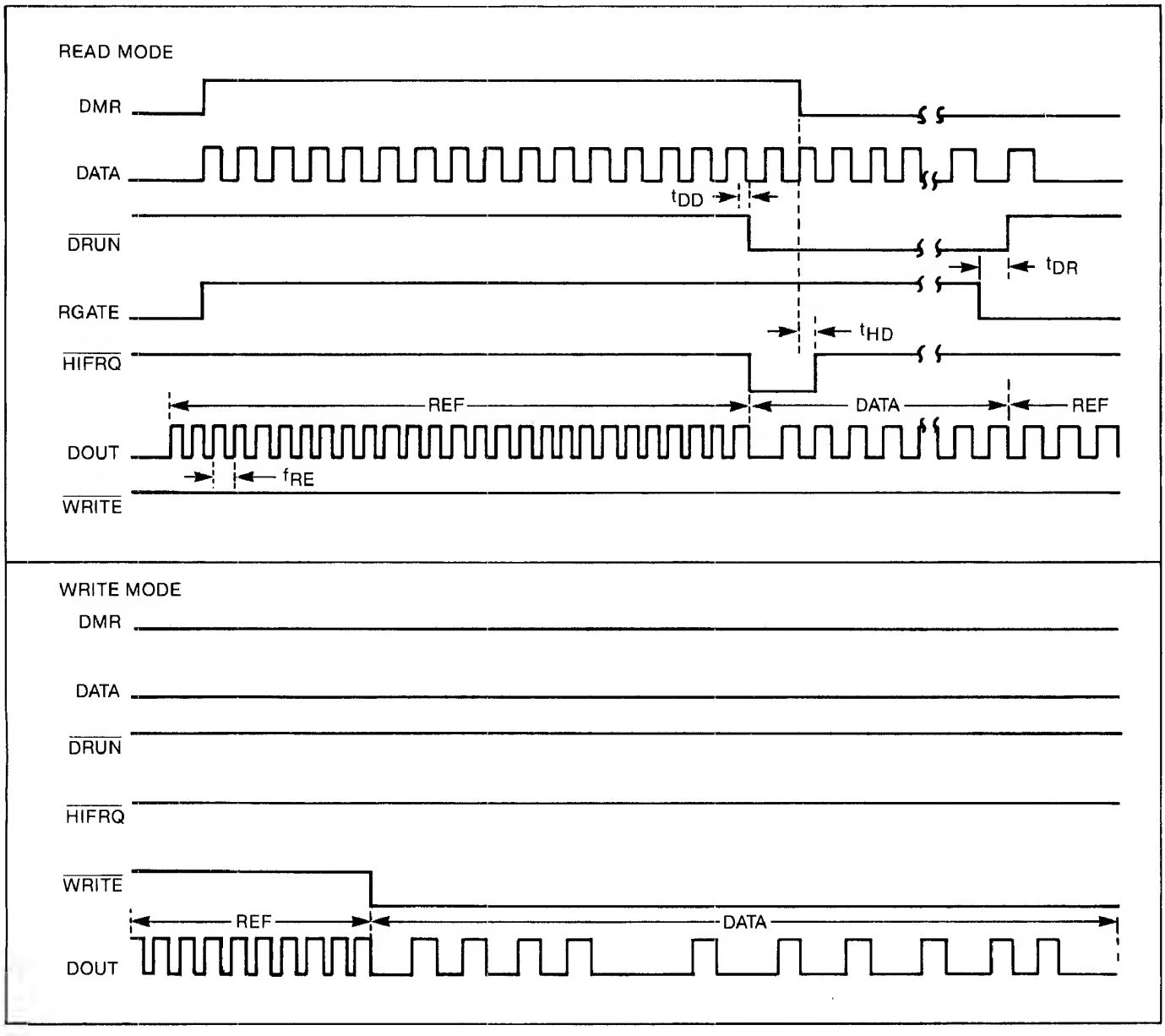
In order to prevent the external VCO from locking onto a harmonic of its operating frequency, REF (pin 2) is provided with a signal twice the data rate that is crystal controlled. With $\overline{\text{WRITE}}$ (pin 6) and RGATE (pin 19) inactive, this signal will appear at DOUT (pin 9). This signal is applied to the pump logic (see above).

The switching function is initiated immediately after RGATE goes true. DMR (pin 18) will be set active as a result of high frequency pulses applied to an external one shot whose pulse width is such that its output is a single stretched pulse. The high frequency pulses are applied to the $\overline{\text{DATA}}$ (pin 1) line and after 16 consecutive pulses, $\overline{\text{DRUN}}$ (pin 8) and $\overline{\text{HIFRQ}}$ (pin 6)

go true. At this point REF is switched out and the DATA stream is switched in and appears at DOUT. DRUN is reset when RGATE goes inactive and HIFRQ goes inactive when DMR goes inactive.

Write Mode

When WRITE (pin 16) goes active, REF is switched out and WDAT (pin 13) will appear at DOUT. Since WDAT is a crystal controlled signal (usually the MFM write data); the VCO is held locked and will not drift (see pump logic above).



AC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DD}	DATA↓ to DRUN↓			170	nSec	
t_{DR}	RGATE↓ to DRUN↑			90	nSec	
t_{HD}	DMR↓ to HIFRQ↑			90	nSec	
f_{RE}	REF frequency		2 TIMES DATA RATE	10	MHz	

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C to 50°C
Voltage on any pin with
respect to V_{SS} . . . . . −0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
Storage Temperature Plastic −55°C to +125°C
Ceramic −55°C to +150°C

NOTE:
Maximum ratings indicate operation when permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All outputs open

NOTE: $\overline{UP}$ and DOWN are open collector outputs and provide 12mA I_{OL} @ .5V.

See page 725 for ordering information.

Printed in U.S.A.

ADVANCE INFORMATION

WD1010 Winchester Disk Controller

FEATURES

- Compatible with most 8- and 16-bit processors
- Data rate up to 5 Mbits per second
- Multiple sector read/write commands
- Unlimited interleave capability
- Automatic formatting
- Software selectable sector size (128, 256, 512, or 1024 bytes per sector)
- CRC generation/verification
- Automatic retries on all errors
- Automatic restore on seek errors
- Single +5V supply
- Provision for external ECC capability

APPLICATIONS

- Seagate ST506, ST512
- Shugart SA1000, SA1100, SA600
- Tandon 600 Series
- Texas Instruments 506
- RMS 500 Series
- Quantum Q2000 Series
- Miniscribe

. . . and others

DESCRIPTION

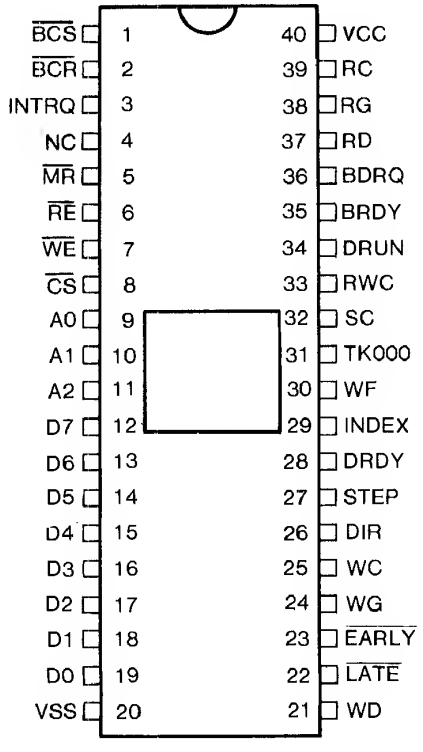
The WD1010 is a MOS/LSI device designed for use with the drives listed above as well as other drives compatible with the SA1000 or ST506 interface. The controller requires only a single +5 volts supply. It is designed to operate with an external sector buffer memory and to interface directly with TTL logic.

The WD1010 is fabricated in NMOS silicon-gate technology and is available in a 40-pin, Dual-in-line ceramic or plastic package.

FUNCTIONAL DESCRIPTION

The WD1010 is software compatible with the WD1000 controller board. Programming is very similar to that of the Western Digital FD179X floppy disk controller.

Data bytes are transferred to or from the buffer every 1.6μsec., with a 5Mbit/sec drive. The buffer may be either the Western Digital WD1510 128x9 FIFO memory (Fig. 1) or a combination of a 256x8 static RAM and a 9 bit resettable counter (Fig. 2). The WD1010 generates control signals to minimize external gating. Buffer to processor transfers are made via programmed I/O or DMA. The controller also generates handshake signals to control DMA operations for multiple sector transfers. The WD1010 interfaces to the Western Digital DM1883 and other DMA controllers.



PIN CONNECTIONS

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
12-19	D7-D0	Data 7 - Data 0	Eight bit bidirectional bus used for transfer of commands, status, and data.
6	$\overline{RE}$	READ ENABLE	Tristate bidirectional line, used as an input for reading the task register and an output when WD1010 is reading the buffer.
7	$\overline{WE}$	WRITE ENABLE	Tristate bidirectional line used as an input for writing into the task register and as an output when the WD1010 is writing to the buffer.
9-11	A0-A2	ADDRESS 0 - ADDRESS 2	These three inputs select the register to receive/transmit data on D0-D7.
8	$\overline{CS}$	CHIP SELECT	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
3	INTRQ	INTERRUPT REQUEST	Active high output which is set to a logic high in the completion of any command.
5	$\overline{MR}$	MASTER RESET	A logic low in this input will initialize all internal logic.
1	$\overline{BCS}$	BUFFER CHIP SELECT	Active low output used to enable reading or writing of the external sector buffer.
35	BRDY	BUFFER READY	This input is used to inform the controller that the sector buffer is full or empty.
2	$\overline{BCR}$	BUFFER COUNTER RESET	Active low output that is strobed by the WD1010 prior to read/write operations.
36	BDRQ	BUFFER DATA REQUEST	This output is set to initiate data transfers to/from the sector buffer.
40	V_{CC}	+ 5 volt	+5V $\pm$ 5% Power supply input.
20	V_{SS}	GROUND	Ground.
4	NC	NO CONNECTION	This pin must be left open by the user.
21	WD	WRITE DATA	This output contains the MFM clock and data pulses to be written on the disk.
25	WC	WRITE CLOCK	4.34 or 5.0 MHz clock input used to derive all internal write timing.
24	WG	WRITE GATE	This output is set to a logic high before writing is to be performed on the disk.
23, 22	$\overline{EARLY}$, $\overline{LATE}$	EARLY, LATE	Precompensation outputs used to delay the WD pulses externally.
37	RD	READ DATA	Data input from the Drive. Both MFM clocks and data pulses are entered on this pin.
39	RC	READ CLOCK	A normal square wave clock input derived from the external data recovery circuits.
38	RG	READ GATE	This output is set to a logic high when data is being inspected from the disk.
39	DRUN	DATA RUN	This input informs the WD1010 when a field of one's or zeroes have been detected.
27	STEP	STEP PULSE	This output generates a pulse for the stepping motor.
26	DIR	DIRECTION	This output determines the direction of the stepping motor.
28	DRDY	DRIVE READY	This input must be at a logic high in order for commands to execute.
30	WF	WRITE FAULT	An error input to the WD1010 which indicates a fault condition at the drive.
31	TK000	TRACK 000	An input to the WD1010 which indicates that the R/W heads are positioned over the outer-most cylinder.

TABLE 1. INTERFACE SIGNALS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
29	INDEX	INDEX PULSE	A logic high on this input informs the WD1010 when the index hole has been encountered.
33	RWC	REDUCED WRITE CURRENT	This output can be programmed to reduce write current on a selected starting cylinder.
32	SC	SEEK COMPLETE	This input informs the WD1010 when head settling time has expired.

PROCESSOR INTERFACE DESCRIPTION

The WD1010 controller interfaces to a host or I/O processor via an 8 bit bidirectional data bus. The buffer memory is also connected to the data bus. The WD1010 is designed for use with buffer memory and external bus transceivers. One anticipated system configuration is shown in Figure 1. In this system, the processor starts a disk operation by writing task information into the register file in the controller. The task information includes the disk cylinder, head, sector numbers, drive number, track number for start of write precompensation, sector size, and number of sectors to be transferred. After the task information has been written, the processor writes the command into the command register. In the case of a write sector command, the processor can then read the controller status register to inspect the buffer data request flag, and write data into the buffer memory. When the buffer becomes full, it activates the BRDY input of the controller. The controller then deactivates the buffer data request (BDRQ) line and activates the $\overline{BCS}$ line. The buffer chip select ($\overline{BCS}$) line is used both for buffer memory control and for disabling the data bus, $\overline{RE}$ and $\overline{WE}$ buffers. The controller thus has a direct bus to the buffer memory which is isolated from the processor data bus. When the buffered data is transferred to disk and the buffer memory is empty, the controller enables the tristate buffers, thus reconnecting the two busses. The processor can then write more data into the buffer memory.

The WD1010 disk controller generates control signals for RAM-counter control, data bus control, ECC processor and DMA control.

TABLE 2. TASK REGISTER FILE

A2	A1	A0	READ	WRITE
0	0	0	Data	Data
0	0	1	Error Flags	Write Precomp Cyl.
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder No. Low	Cylinder No. Low
1	0	1	Cylinder No. High	Cylinder No. High
1	1	0	SDH	SDH
1	1	1	Status	Command

TABLE 3. SDH REGISTER

SECTOR EXTENSION	SECTOR SIZE		DRIVE* NUMBER		HEAD* NUMBER		
BIT 7	6	5	4	3	2	1	0
1 = ECC 0 = CRC	1 0 0 1	1 0 1 0	128 byte data field 256 byte data field 512 byte data field 1024 byte data field				

*Drive Number and Head Number must be externally decoded and latched.

DRIVE INTERFACE DESCRIPTION

The WD1010 disk controller is designed to interface to SA1000 Winchester disk drives. Winchester drives with similar interfaces, such as the Seagate Technology ST506, can also be controlled.

The WD1010 contains MFM encoder/decoder, address mark detector, and high speed shift register circuitry. Signals are provided to control write precompensation and write splice avoidance. External circuitry must provide a phase locked MFM read clock and high frequency detection. Figure 1 shows a typical controller-drive interface for a system with two Winchester disk drives.

WD1010 inputs are TTL compatible unless otherwise noted. WD1010 outputs will drive one TTL unit load.

STATUS BIT DESCRIPTION

Busy — Active when controller is accessing the disk. Activated by start of command (writing into command register). Deactivated at end of all except read sector. For read sector, Busy is deactivated when a sector of data has been transferred to buffer.

Drive Ready — Normally reflects the state of DRDY pin. After an error interrupt, the state of DRDY is frozen until the status register is read. The DRDY bit then reflects the state of the DRDY pin. An interrupt is generated when reset.

Write Fault — Reflects the state of the WF pin. An interrupt is generated when set.

Seek Complete — Reflects the state of the SC pin.

Data Request — Reflects the state of the BDRQ pin. When active, indicates that a buffer data transfer is desired. The data request flag is used for programmed I/O while the BDRQ pin is used for DMA controlled I/O.

Command in Progress — Indicates that a command is in progress.

Error — Indicates that a bit in the error register has been set.

ERROR BIT DESCRIPTION

Bad Block — A bad block address mark has been detected when trying to read or write that sector.

Data Field CRC Error — An error in the data field has been detected. The sector can be re-read to attempt recovery from a soft error. The data contained in the buffer can be read but contains errors.

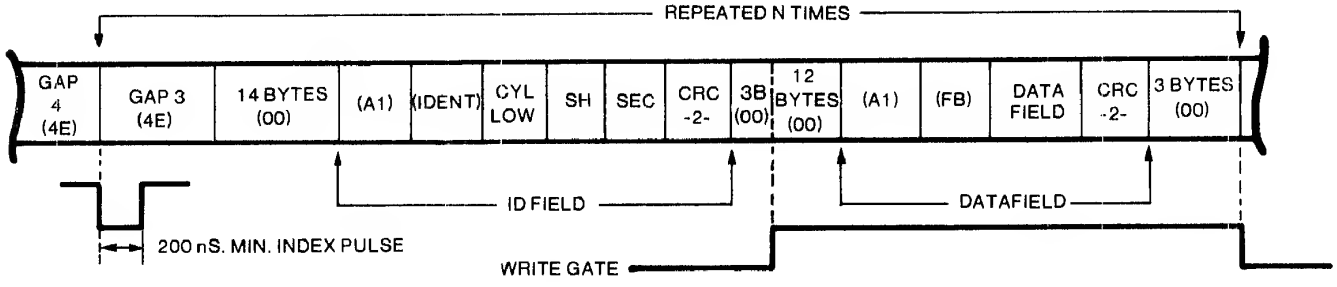
ID Not Found — Occurs when cylinder, head, sector, or size parameters cannot be found after 16 index pulses have been encountered.

TK000 Error — Occurs when track 0 not found in a Restore command after 1024 stepping pulses.

Aborted Command — Set if command was started and one of the following conditions occurred:

1. Drive not ready
2. Write fault
3. Seek complete not active within 16 index pulses
4. Illegal command code

Data AM Not Found — During a read command, the ID field for the desired sector has been found, but the data field address mark was not found. The data AM should be found within 15 bytes after the ID field. Refer to Figure 3 for track format.



NOTE:

1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high. These values are:
   FF = 0 to 255 cylinders
   FF = 256 to 511 cylinders
   FC = 512 to 767 cylinders
   FD 768 to 1023 cylinders
6) GAP 3 length is programmable and may range from 3 bytes to 255 bytes.

FIGURE 3
TRACK FORMAT

TABLE 4. STATUS/ERROR REGISTERS

BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	BUSY	Bad Block
6	DRIVE READY	Data Field CRC
5	WRITE FAULT	Reserved (= 0)
4	SEEK COMPLETE	ID Not Found
3	DATA REQUEST	Reserved (= 0)
2	RESERVED (= 0)	Aborted Command
1	COMMAND IN PROGRESS	TK000 Error
LSB 0	ERROR	Data AM Not Found

TABLE 5. COMMAND REGISTER

COMMAND	MSB 7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	D	M	0	0
WRITE SECTOR	0	0	1	1	0	M	0	0
SCAN ID	0	1	0	0	0	0	0	0
WRITE FORMAT	0	1	0	1	0	0	0	0

D = 1 for DMA; 0 for Programmed I/O
M = 1 for multiple sector read or write

R3 R2 R1 R0 = 0000 : Step time = 20 us
0001 : Step time = .5 ms
0010 : Step time = 1.0 ms
0011 : Step time = 1.5 ms
1111 : Step time = 7.5 ms
for 5 MHz write clock

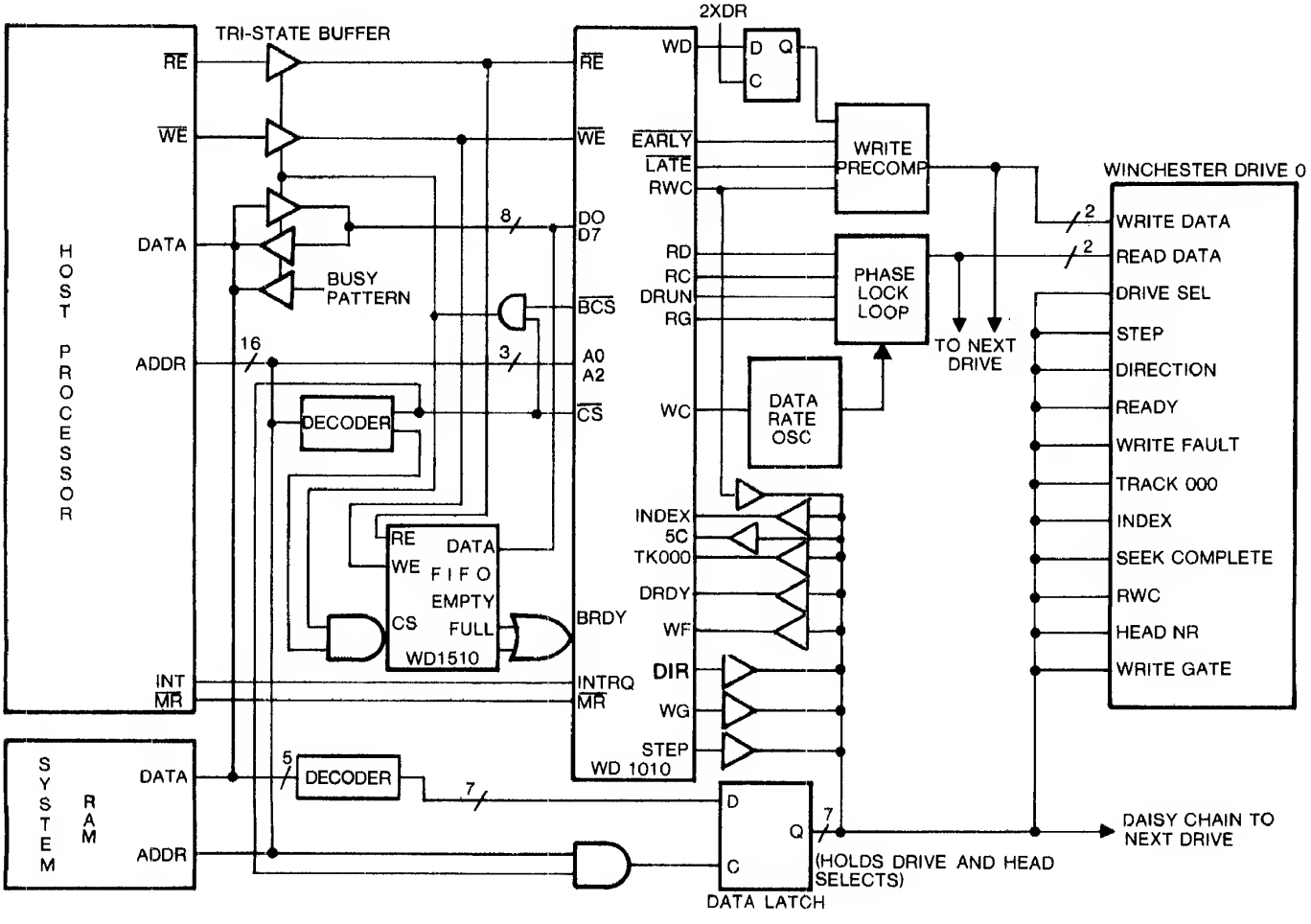


FIGURE 1.

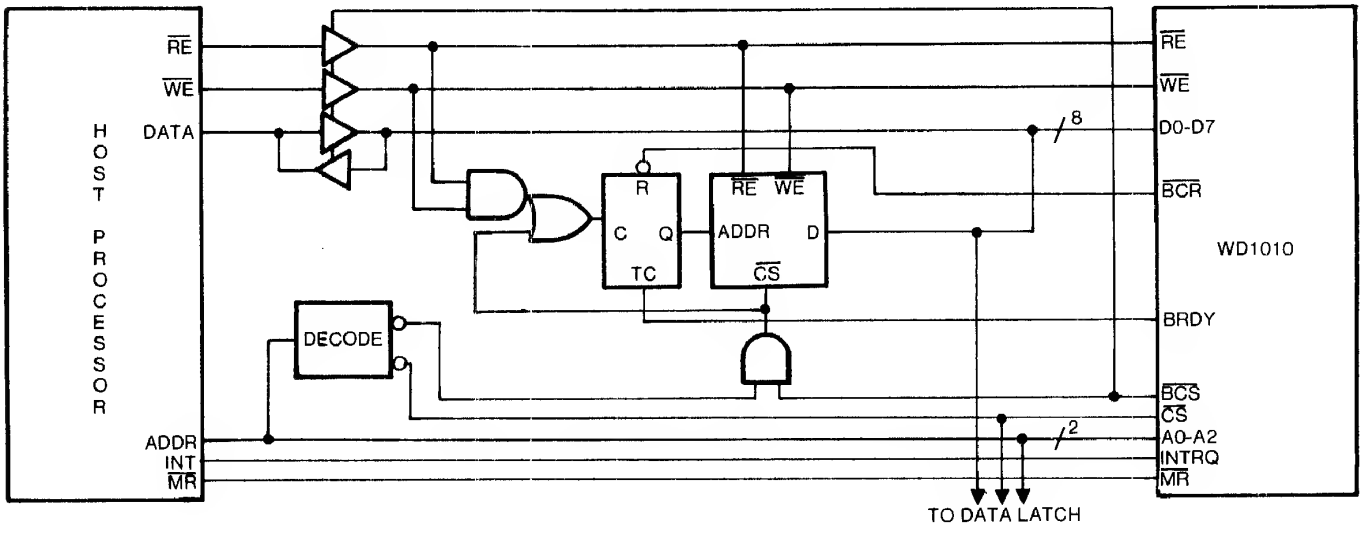


FIGURE 2.

See page 725 for ordering information.

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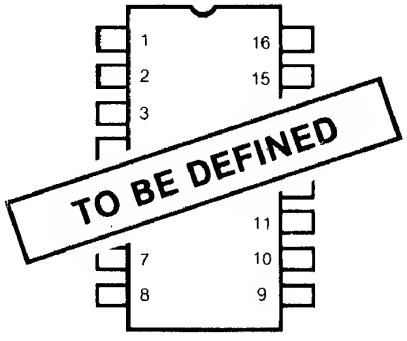
ADVANCE INFORMATION

WD1011 Winchester Data Separator Device

FEATURES

- 4.34 OR 5.0 MBIT/SEC DATA RATE
- INTERNAL CRYSTAL OSCILLATOR
- SINGLE +5V SUPPLY
- FM OR MFM OPERATION
- COMPATIBLE WITH THE WD1010
- WRITE CLOCK GENERATOR
- HIGH FREQUENCY DETECTION



PIN DESIGNATION

GENERAL DESCRIPTION

The WD1011 Winchester Data Separator has been designed to replace the complex analog/digital circuitry required for data recovery by Winchester disk drives. Directly interfacing to the WD1010 Winchester Controller device, an on-chip crystal oscillator allows operation of 4.34 Mbit/sec or 5.0 Mbit/sec transfer rates. In addition to data recovery, the device provides Write Clock signals for the WD1010 as well as high frequency detection for pre-amble search. Output levels on data pins swing close to the supply rails for increased noise immunity and to minimize layout restrictions.

The WD1011 operates from a single 5 volt supply and is available in a 16 pin plastic or ceramic Dual-in-Line package.

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1012 Write Precompensation Device

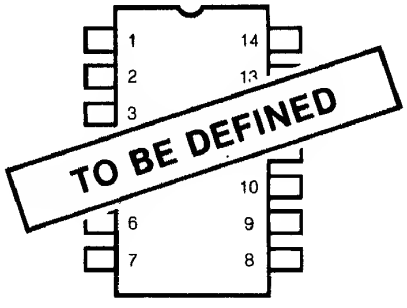
FEATURES

- DIRECT INTERFACE TO THE WD1010
- 12 NS. TYP. DELAY FROM EARLY
- PROVIDES TIMCLK FOR SA1000 TYPE DRIVES
- SINGLE +5V SUPPLY
- TTL COMPATIBLE INPUT/OUTPUTS
- COMPANION CHIP TO THE WD1011 DATA SEPARATOR

GENERAL DESCRIPTION

The WD1012 Write Precompensation device provides delayed data necessary for inner cylinder recording on Winchester disk drives. It is a companion chip to the Western Digital WD1010, utilizing signals from both the WD1010 and WD1011 data separator device. The WRITE DATA output, as well as EARLY, LATE, and RWC are applied to produce a pre-determined bit shift. Assertion of EARLY or LATE will cause a 12 ns. typ. shift of data based upon the precompensation algorithm internal to the WD1010. In addition, a divide-by-sixteen timing clock output is available for use by the SA1000 and other drives requiring a TIMCLK input.

The WD1012 operates from a single 5 volt supply and is available in a 14 pin plastic or ceramic package.



PIN DESIGNATION

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1014 Buffer Manager/Error Correction Device

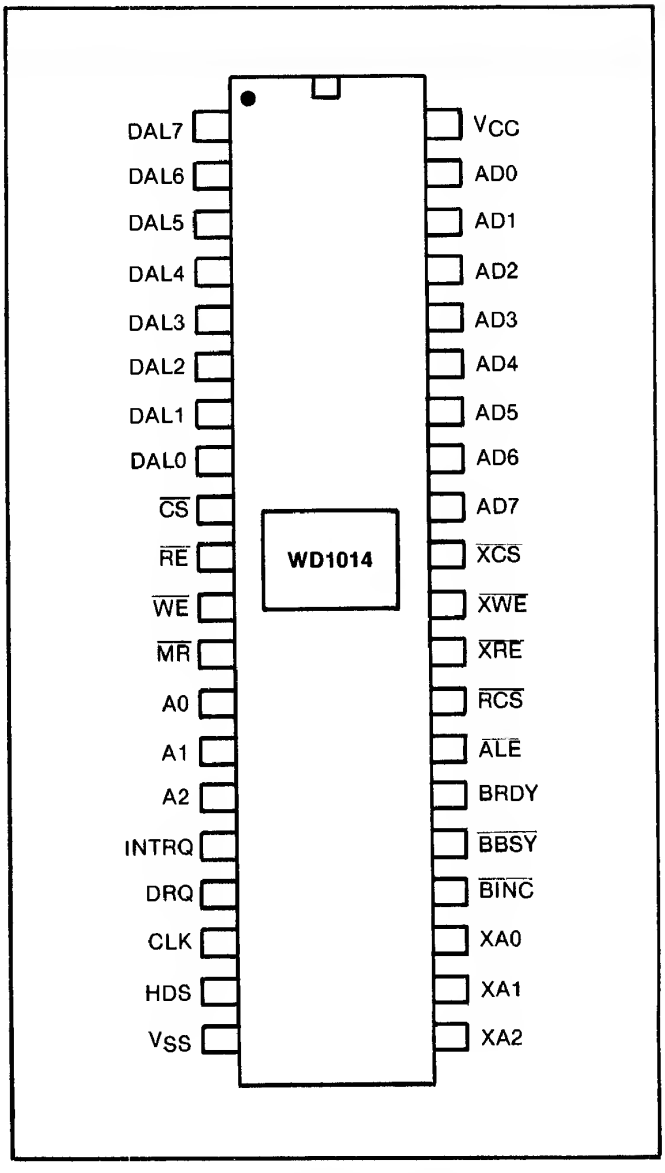
FEATURES

- DIRECT INTERFACE TO THE WD1010
- 32 AND 56 BIT ECC POLYNOMIALS
- 128, 256, 512, OR 1024 BYTE SECTORS
- BUFFER SIZE UP TO 32K BYTES
- CONTROL FOR 4 DRIVES/8 HEADS EACH
- AUTOMATIC RETRY ON ECC ERRORS
- TRANSPARENT ECC CORRECTION
- MULTI-SECTOR READ/WRITE CAPABILITY
- DMA OR PROGRAMMED I/O OPERATION
- 8-BIT TRI-STATE DATA BUS
- EXECUTES 11 MACRO-COMMANDS
- SINGLE +5V SUPPLY

GENERAL DESCRIPTION

The WD1014 is a single chip Buffer Manager/ECC device designed for use with the Western Digital Corp. WD1010 Hard Disk Controller. The device implements all of the logic required for a variable length sector buffer, ECC correction and Host interface circuitry. Use of the BMEC greatly reduces the complexity of the interface design, device count, board size requirements and increases system reliability.

The WD1014 operates from a single +5V supply and is available in a 40 pin plastic or ceramic Dual-in-Line package.



PIN DESIGNATIONS

PIN NUMBER	SYMBOL	DESCRIPTION
1-8	DAL7-0	Data Access Lines. Commands, status, and data to and from buffer are transferred over this tristate bidirectional data bus controlled by the host. DAL7 is MSB.
9	$\overline{CS}$	Chip Select must be active for all communications with the BMEC.
10	$\overline{RE}$	Read Enable. For reading data and status information from the BMEC.
11	$\overline{WE}$	Write Enable. For writing commands and data to the BMEC.
12	$\overline{MR}$	Master Reset. Initializes the BMEC and clears the status flags when activated.
13-15	A0-2	Address inputs. Used to select task file registers and data buffer. A2, A1, A0 = 000 selects buffer. A2 is MSB.
16	INTRQ	INTerrupt ReQuest. Activated whenever a command has been completed. It is reset when the status register is read, or when a new command is loaded via DAL7-0.
17	DRQ	Data ReQuest. Set whenever the buffer contains data to be read by the host or is awaiting data to be written by the host.
18	CLK	Clock signal input used for all internal timing.
19	HDS	Head & Drive Select for setting HS0-3 and DS1-4.
20	V_{SS}	GROUND
21-23	XA2-0	These address lines are used to address the disk controller when $\overline{XCS}$ = 0.
24	$\overline{BCINC}$	Buffer Counter INCrement. Increments the external buffer counter. Each negative transition is a one byte count.
25	$\overline{BBSY}$	Buffer BuSY. Signals the BMEC that the buffer is being accessed by the disk controller. It is also used to control AD0-7 bus switching and tristate $\overline{XWE}$, and $\overline{XRE}$ when it is active.
26	BRDY	Buffer ReaDY output. Signals the disk controller when the buffer memory is ready for controller data transfers. It is active when the buffer memory is full or empty.
27	$\overline{ALE}$	Address Latch Enable. Used to set the external buffer address whenever the buffer is not being accessed by the WD1010 processor.
28	$\overline{RCS}$	Ram Chip Select. Asserted when the BMEC or host accesses the external buffer.
29	$\overline{XRE}$	Tristate line activated only when $\overline{BBSY}$ = high. When $\overline{XCS}$ is low, information is read from the selected WD1010 task files registers. When $\overline{RCS}$ is low, data is read from the buffer.
30	$\overline{XWE}$	Tristate line activated only when BBSY = high. When $\overline{XCS}$ is low, command or task file information is written into the disk controller. When $\overline{RCS}$ is low data is written into the buffer.
31	$\overline{XCS}$	This Chip Select is used to access the disk controller.
32-39	AD7-0	Address or Data bus shared by the buffer, BMEC and the WD1010. While ALE is active a new buffer address is latched in an external counter, where AD7 = A14 and AD0 = A7. This allows buffer sizes from 128 bytes to 32K bytes.
40	V_{CC}	+5 ± 5% volt power supply.

FUNCTIONAL DESCRIPTION

The BMEC is designed to interface directly with industry standard static RAM chips and common TTL/LS latches and counters. The sector buffer, an integral part of the WD1010 system architecture, is addressed by a multiplexed data/address bus (AD0-7), which is also shared by the WD1010 and drive/head control latches. The WD1014 manages the external sector buffer so that it can support all WD1010 sector sizes in single and multiple sector operations. All buffer control signals required by the WD1010 are produced by the BMEC so that no external logic is required to interface the WD1010 to the BMEC.

During sector reads and writes, the BMEC produces an Error Correction Code (ECC) as data is transferred to and from the buffer. The user may select either a 32 or 56 bit polynomial depending upon his needs. Errors are detected and corrected without intervention by the host. The BMEC controls all retries on data ECC errors for the host as well. Corrected errors are reported as a status to the host. Uncorrectable errors are reported by setting the error bit in the status register with the appropriate descriptor bit set in the error register.

TASK FILE

The task file is a set of registers which contain commands, status, track, sector and other task information. Nine registers are accessed via A2 to A0 during read and write modes. Depending on the command from the host and the status of the system, the proper information is stored to or read from the task file.

A2	A1	A0	READ	WRITE
1	1	1	Status	Command
0	0	1	Error flags	Write Precomp Cylinder
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Number (low)	Cylinder Number (low)
1	0	1	Cylinder Number (high)	Cylinder Number (high)
1	1	0	S D H*	S D H*

*S D H bytes specifies sector size, drive number and head number.

The SDH register is coded as follows:

Bit 7 (MSB) is set for a 7 byte sector extension (used for ECC bytes).

Bits 6 and 5 contain the sector size.

The possible sector sizes and their selection codes are:

BIT 6	BIT 5	SECTOR SIZE
1	1	128 byte data field
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field

Bits 4 and 3 specify Drive Number. These bits are decoded internally and latched externally to perform the select function.

Bits 2, 1 and 0 specify Head Number.

COMMAND REGISTER

The command register is accessed by writing into register 7. All other task information should be loaded into the task file before loading the command register. Command execution starts immediately after the command register is loaded and subsequent register loads are ignored until the command is done. The commands are as follows:

COMMAND	BIT CODE MSB 7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R_0
Seek	0	1	1	1	R3	R2	R1	R_0
Read Sector	0	0	1	0	D	M	0	E
Write Sector	0	0	1	1	0	M	0	E
Scan ID	0	1	0	0	0	0	0	0
Write Format	0	1	0	1	0	0	0	0
Read Copy	1	0	1	0	0	M	0	E
Write Copy	1	0	1	1	0	M	0	E
Read Long	0	1	1	0	D	0	1	E
Write Long	0	1	1	1	D	0	1	E
Set Parameters	1	1	0	1	0	0	0	0

D = 1: Interrupt for DMA mode
D = 0: Interrupt for programmed I/O mode
M = 1: Multiple Sector Read or Write
E = 1: Select 56 bit ECC polynomial
E = 0: Select 32 bit ECC polynomial
R3 R2 R1 R0 = 0000 : Step time = 20μs
0001 : Step time = .5ms
0010 : Step time = 1.0ms
0011 : Step time = 1.5ms
:
:
1111 : Step time = 7.5ms for 5 MHz write clock

THE STATUS AND ERROR REGISTERS

The Status Register indicates to the host the status of the system. If the Error bit in the Status Register is set, one or more bits in the Error Register will be set. The meaning of the these bits is shown below:

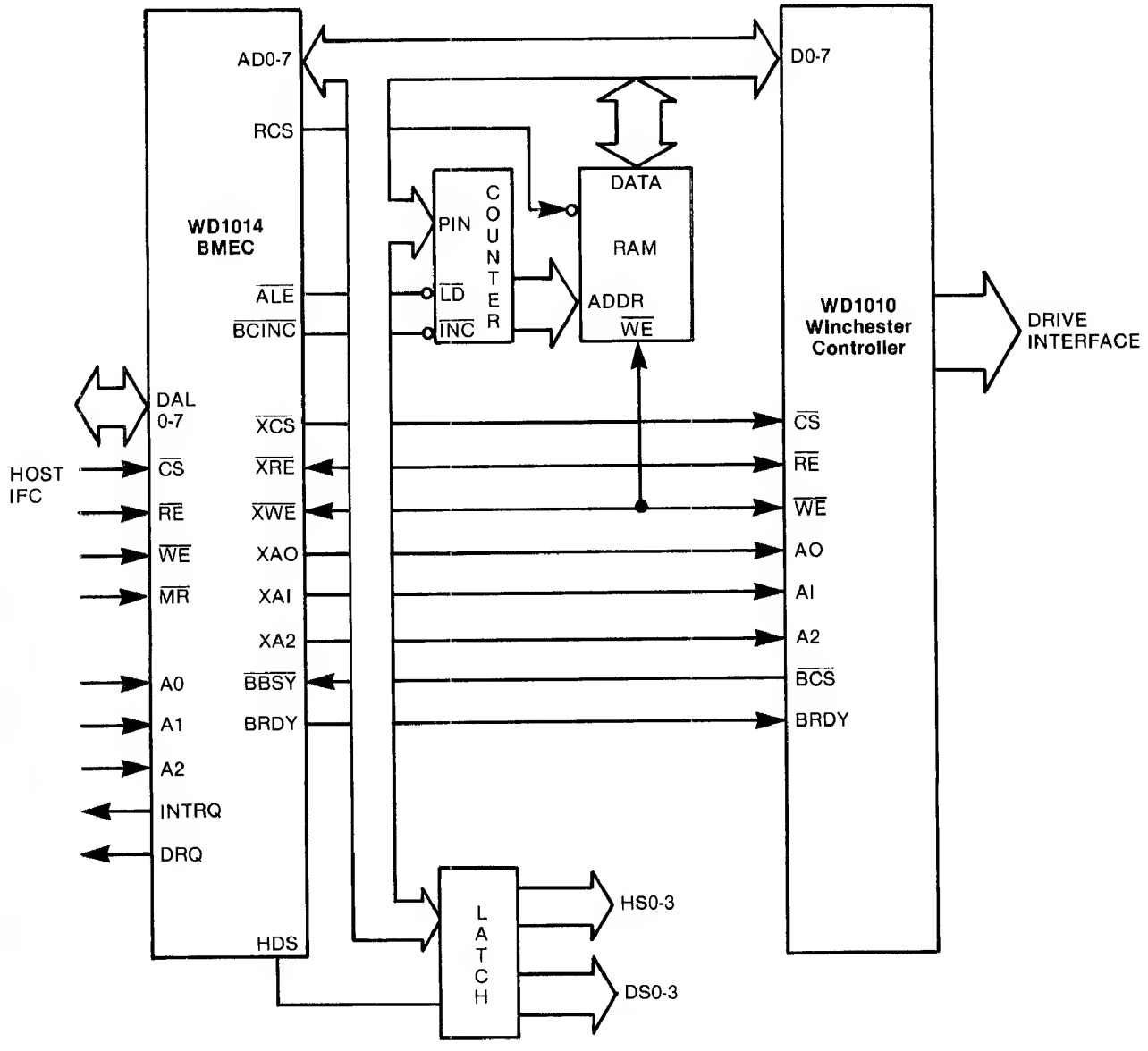
BIT	STATUS REGISTER	ERROR REGISTER
MSB 7	Busy	Bad Block Detect
6	Drive ready	Uncorrectable
5	Write fault	CRC Error — ID Field
4	Seek complete	ID Not Found
3	Data request	——
2	Data Error Corrected	Aborted Command
1	Command in progress	TR000 Error
LSB 0	Error	DAM Not Found

COMMAND DESCRIPTIONS

The BMEC passes on all information between the host and the WD1010. Some commands are modified by the BMEC and some are simply echoed. The following is a list of the commands and their formats and descriptions.

COMMAND	FORMAT	DESCRIPTION
RESTORE	0 0 0 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SEEK	0 1 1 0 R3 R2 R1 R0	Pass on task information and command and initiates a read status after the command is completed. The command is echoed. Stepping rate (R0-R3) is set.
SCAN ID	0 1 0 0 0 0 0 0	Passes command to WD1010 which scans ID headers on current track. Updates cylinder number in task file and command and initiates a read status after the command is completed. The command is echoed.
READ SECTOR	0 0 1 0 D M 0 E	Write the buffer with data from WD1010. If ECC is enabled, ECC bytes are recomputed by the BMEC. After the buffer is full, the recorded ECC bytes are compared to the generated bytes to generate the syndrome bytes. If the syndrome is non-zero, errors have occurred and error correction is invoked by the BMEC. If the error is not correctable the BMEC retries the sector read. If the data is correctable the BMEC corrects the data and passes the data in the buffer to the host. Read status is requested by the BMEC and is sent from the WD1010 to the host. If, after a specified number of retries, the error is still uncorrectable, the BMEC sends an error status to the host along wtih the status from the WD1010.
WRITE SECTOR	0 0 1 1 0 M 0 E	Write the buffer with data bytes from the host. Pass the task information and command to the WD1010. The WD1010 seeks track if necessary, then writes the sector from the buffer to disk. Generate the ECC polynomial, selected by E, as the buffer is written to disc. Write the total number of sectors specified by the sector count if M = 1 in format. If M = 0 then the sector count is ignored and only one sector is written. After the sector data is written to the disc, the BMEC sends the WD1010 the ECC bytes. The BMEC requests status from the WD1010 and passes on this information to the host at the host's request.
READ LONG	0 1 1 0 D 0 1 E	Similar to Read Sector except the ECC operation producing a syndrome is inhibited in the BMEC. Instead, the BMEC copies the recorded ECC bytes from disc and passes them unaltered to the host.
WRITE LONG	0 1 1 1 D 0 1 E	The Write Long command functions similarly to the Write Sector command except the ECC operation of computing the ECC word is inhibited in the BMEC. Instead, the BMEC accepts a 32, or 56 bit appendage from the host and passes it unaltered to the WD1010 to be written on the disc after the data.
WRITE COPY	1 0 1 1 0 M 0 E	The Write Copy command is similar to the Write Sector command, except the BMEC does not send a data request (DRQ) to the host at the beginning of the command. The BMEC assumes it has a full buffer to write to the disc. The buffer could have been filled by another device other than the host, such as a back-up tape or data from another disc. This commands allows the copying of data from one disc to another with minimal host intervention.

COMMAND	FORMAT	DESCRIPTION
READ COPY	1 0 1 0 0 M 0 E	The Read Copy command is similar to the Read Sector command, except the BMEC does not send a data request (DRQ) to the host at the end of the command. This command, when used with the Write Copy command, allows the copying of data from one disk to another with minimal host intervention.
SET PARAMETERS	1 1 0 1 0 0 0 0	The buffer size parameter is specified by the value held in the sector size task register. The buffer size corresponds to the sector size task register value multiplied by 128. (E.G. if the sector size task register value = 1, then it specifies a buffer size of 128 bytes. A 32768 (32K) byte length buffer is specified by a sector size register value = 0.)



WD1010/WD1014 WINCHESTER CONTROLLER

See page 725 for ordering information.

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ADVANCE INFORMATION

WD1050 SMD Controller/Formatter

FEATURES

- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- HARD SECTOR FORMAT
- TTL COMPATIBLE INPUT/OUTPUTS
- SINGLE 5V SUPPLY
- 64 PIN JEDEC CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES

DESCRIPTION

The WD1050 SMD controller/formatter is a MOS/LSI device designed to interface an SMD compatible rigid disk drive to a host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on all inputs and outputs, with interface capability for 8 or 16 bit data busses.

The WD1050 contains a powerful set of macro-commands for read/write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 64 pin JEDEC chip-carrier package.

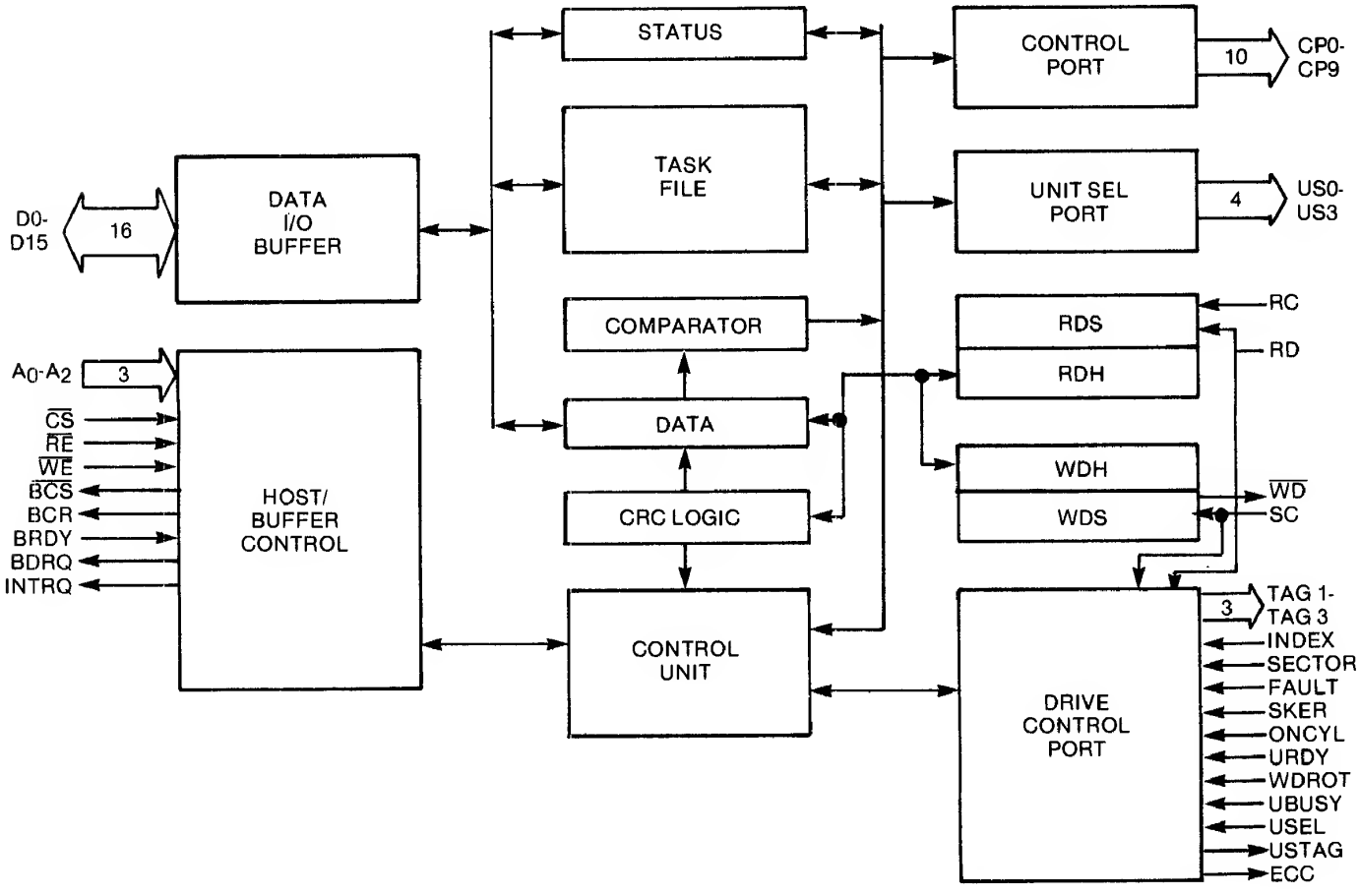


Figure 1 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	V_{CC}	V_{CC}	+5V ± 5% power supply input
2	READ ENABLE	$\overline{RE}$	Tri-state bidirectional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
3	WRITE ENABLE	$\overline{WE}$	Tri-state bidirectional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
4	CHIP SELECT	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals.
5-7	ADDRESS 0→2	A0→A2	These three inputs select a task file register to receive/transmit data.
8-23	DATA BUS 0-15	D0-D15	Sixteen bit bidirectional bus used for transfer of commands, status, and data.
24	WRITE DATA	$\overline{WD}$	Open Drain, NRZ data output which is synchronized to the Servo Clock input.
25	READ CLOCK	RC	Input clock from the drive which is synchronized with the Read Data Input.
26	SERVO CLOCK	SC	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
27	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
28	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
29	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
30	UNIT SELECT	USEL	Active high output pulse used to strobe US0-US2 lines.
31	UNIT READY	URDY	Active high input used to inform the WD1050 of a READY condition on a selected drive. If this line is made inactive during any command (except RTZ or FAULT CLEAR), current command execution is terminated.
32	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
33	GROUND	V_{SS}	Ground.
34	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if fault is made active during any command. Only the FAULT CLEAR command may be issued while this line is ascerted.
35	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
36	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over the desired cylinder.
37	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	ERROR CORRECTION	ECC	Active high output used to synchronize external ECC logic to the Data Field.
39	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on US0-US3 lines.
40-42	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 — Cylinder address TAG2 — Head/Volume select TAG3 — Control Tag
43-46	UNIT SELECT 0-3	US0-US3	These four outputs reflect the contents of the unit address field of the task file, and are used to select one of four drives.
47-56	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
57	BACK-BIAS	V_{BB}	Substrate generator. Must be left open by the user.
58	BUFFER CHIP SELECT	$\overline{BCS}$	Active low output used to enable reading or writing to the external buffer.
59	BUFFER COUNTER RESET	BCR	Active low output that is strobed prior to read/write commands. Used to clear an external buffer counter.
60	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
61	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is full or empty.
62	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word.
63	MASTER RESET	$\overline{MR}$	Active low input used to initialize the WD1050, usually after a power-up condition.
64	CLOCK	CLK	2 MHz Master Clock from which all timing is derived.

ORGANIZATION

The Block Diagram of the WD1050 is shown in Figure 1. Data transfers to and from the host, as well as the sector buffer, are transferred via the D0-D15 lines. An internal control unit is used to process all commands and generate drive control signals in the SMD protocol. With the use of an external sector buffer, the WD1050 directly transfers data from the buffer to the read/write lines by the host/buffer control logic. Four buffer control signals are used to manipulate the data off-line from the host processor.

TASK FILE

Inidividual registers within the task file are accessed via the A_2-A_0 lines in conjunction with either Read Enable ($\overline{RE}$) or Write Enable ($\overline{WE}$) signals. Chip Select ($\overline{CS}$) must also be made active during an $\overline{RE}$ or $\overline{WE}$ sequence.

The MSB of the address lines (A_2) can be used for 8-bit operations when interfacing to 8-bit microprocessors. When $A_2 = 0$, 16 bit programming is in effect as shown in Figure 1. When A_2 is toggled, 8-bit selection is enabled, with data entered on D8-D15 illustrated in Table 2.

TABLE 1 TASK FILE (16 BIT PROGRAMMING)

R/W		ADDRESS			TASK FILE REGISTER	
$\overline{WE}$	$\overline{RE}$	A2	A1	A0	D_{15} D_8	D_7 D_0
✓	✓	0	0	0	Head Number	Sector Address
✓	✓	0	0	1	Upper Cylinder	Lower Cylinder
✓	✓	0	1	0	Sector Count	Section Length/Unit Address
✓		0	1	1	Upper Command	Lower Command
	✓	0	1	1	Upper Status	Lower Status

TABLE 2 TASK FILE (8 BIT PROGRAMMING)

R/W		ADDRESS			TASK REGISTER
$\overline{WE}$	$\overline{RE}$	A2	A1	A0	D_7 D_0
✓	✓	1	0	0	Head Number
✓	✓	0	0	0	Sector Address
✓	✓	1	0	1	Upper Cylinder
✓	✓	0	0	1	Lower Cylinder
✓	✓	1	1	0	Sector Count
✓	✓	0	1	0	Sector Length/Unit Address
✓		1	1	1	Upper Command
✓		0	1	1	Lower Command
	✓	1	1	1	Upper Status
	✓	0	1	1	Lower Status

COMMAND SET

The WD1050 can execute eight macro-commands. The appropriate task registers are first loaded with parameter information, then the macro-command is written into the command register. Table 3 shows the eight commands, plus a summary of the various flags used to modify the execution of each command. The STATUS Register, illustrated in Table 4 allows the host to monitor key signals and command progress. Note that the status register is a "Read-Only" register, while the command register is a "Write Only" register. Both these registers share the same address, and are differentiated by the ascertion of either $\overline{RE}$ or $\overline{WE}$.

When programmed for the 8-bit mode, two consecutive reads must be accomplished to fetch the entire status word from the task file. When $A_2 = 1$, status bits D8-D15 are read; when $A_2 = 0$, status bits D0-D7 are read.

COMMAND	LSB				COMMAND REGISTER BITS											MSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	0	0	0	0	0	0	0	I	0	0	0	0	U	S	E	L
Return to Zero	0	0	0	1	V	L	O	I	0	0	0	M	U	S	E	L
Seek Cylinder	0	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	L
Read ID Field	0	0	1	1	0	L	O	I	Z	C	H	M	U	S	E	L
Read Sector	0	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	L
Write Sector	0	1	0	1	0	L	O	I	Z	C	H	M	U	S	E	L
Format	0	1	1	0	0	P	O	I	Z	C	H	M	U	S	E	L
Verify	0	1	1	1	0	P	O	I	Z	C	H	M	U	S	E	L

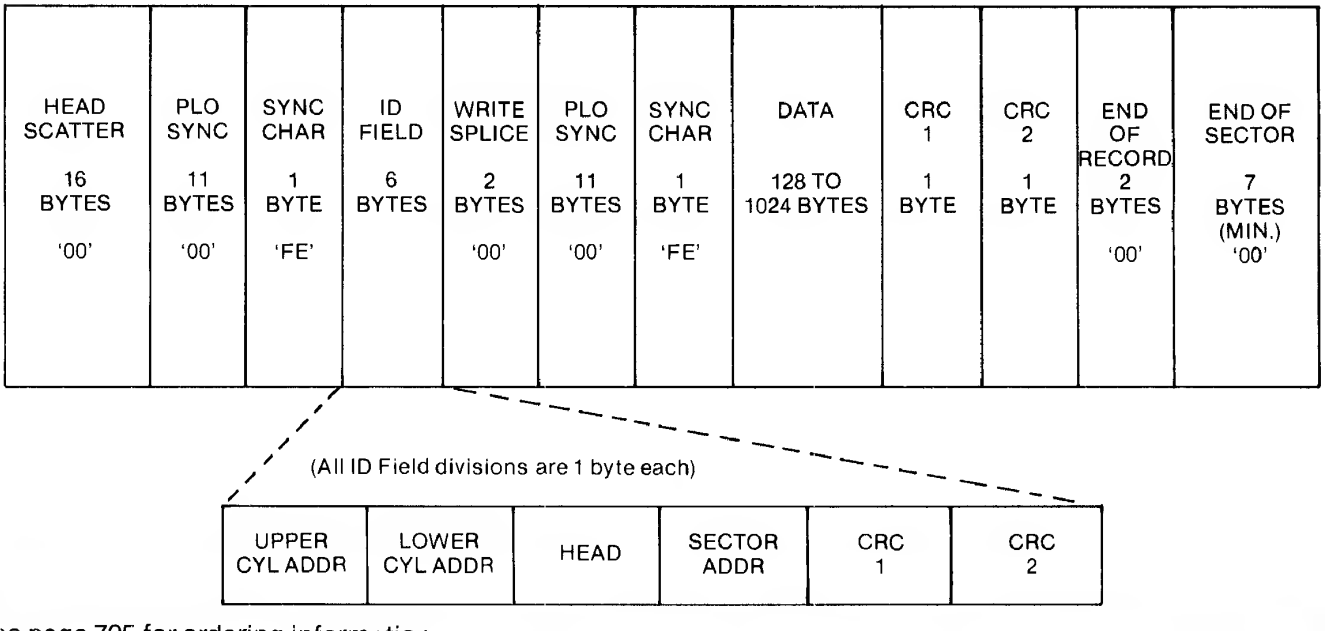
TABLE 3 COMMAND AND FLAG SUMMARY

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head change
L = Logical Sectoring	C = Cylinder Addr
P = Programmable Sectors	H = Head selection
O = On Cylinder	M = Marginal data recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
L = Unit Deselect/Late	S = Priority Sel/Servo Plus

TABLE 4 STATUS WORD SUMMARY

	BIT	STATUS DESCRIPTION
UPPER	15	BUFFER CHIP SELECT STATUS
	14	COMMAND IN PROGRESS
	13	UNIT BUSY
	12	UNIT SELECTED
	11	WRITE PROTECT
	10	UNIT READY
	9	ON CYLINDER
	8	SEEK ERROR
LOWER	7	BUFFER CHIP SELECT STATUS
	6	FAULT CONDITION
	5	BUFFER DATA REQUEST STATUS
	4	NOT USED
	3	DATA FIELD CRC ERROR
	2	DATA SYNCH MARK NOT FOUND
	1	ID CRC ERROR
	0	ID NOT FOUND

FIXED SECTOR FORMAT



See page 725 for ordering information.

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